L Number	Hits	Search Text	DB	Time stamp
1	0	(spice and power adj converter).ab.	USPAT; US-PGPUB	2004/06/03 13:09
2	0	((spice) and (power adj converter)).ab.	USPAT; US-PGPUB	2004/06/03 13:10
3	11	(spice) and (power adj converter)	USPAT; US-PGPUB	2004/06/03 13:17
4	7279	power adj converter	USPAT; US-PGPUB	2004/06/03 13:18
5	475	(power adj converter) and layout	USPAT; US-PGPUB	2004/06/03 13:18
6	268	(power adj converter) and pcb	USPAT; US-PGPUB	2004/06/03 13:19
7	57	((power adj converter) and layout) and ((power adj converter) and pcb)	USPAT; US-PGPUB	2004/06/03 13:19
8	12239	dc adj dc	USPAT; US-PGPUB	2004/06/03 13:19
9	33	(((power adj converter) and layout) and ((power adj converter) and pcb)) and (dc adj dc)	USPAT; US-PGPUB	2004/06/03 13:19
-	257227	converter	USPAT; US-PGPUB	2004/06/03 06:51
-	152	bump adj grid	USPAT; US-PGPUB	2004/06/03 06:53
-	197555	simulat$	USPAT; US-PGPUB	2004/06/03 06:54
-	502871	model$	USPAT; US-PGPUB	2004/06/03 06:55
-	1848	(dc adj dc) and (power adj converter)	USPAT; US-PGPUB	2004/06/03 06:55
-	1282	(power adj converter) and model$	USPAT; US-PGPUB	2004/06/03 07:20
-	27	(bump adj grid) and model$	USPAT; US-PGPUB	2004/06/03 09:55
-	17	(dc adj dc) same (power adj converter) same model$	USPAT; US-PGPUB	2004/06/03 13:07

L Number	Hits	Search Text	DB	Time stamp
1	12239	dc adj dc	USPAT; US-PGPUB	2004/06/03 06:49
2	257227	converter	USPAT; US-PGPUB	2004/06/03 06:51
3	7279	power adj converter	USPAT; US-PGPUB	2004/06/03 06:51
4	152	bump adj grid	USPAT; US-PGPUB	2004/06/03 06:53
5	197555	simulat$	USPAT; US-PGPUB	2004/06/03 06:54
6	502871	model$	USPAT; US-PGPUB	2004/06/03 06:55
7	1848	(dc adj dc) and (power adj converter)	USPAT; US-PGPUB	2004/06/03 06:55
8	27	(bump adj grid) and model$	USPAT; US-PGPUB	2004/06/03 06:56
9	1282	(power adj converter) and model$	USPAT; US-PGPUB	2004/06/03 07:20
10	17	(dc adj dc) same (power adj converter) same model$	USPAT; US-PGPUB	2004/06/03 07:20

Cart.

(SPICE and power adj converter) ab. IEEE. google.

(Power adj Converter) and layout.

(" ") " PCB.

H1 ANN (P) AD< 20010328

"Power Converter" "Layout" "design."

Power Converter and Library

```
Set     Items   Description
S1        182   AU='GAUTHIER C' OR AU='GAUTHIER C R' OR AU='GAUTHIER CLAUD-
                 E' OR AU='GAUTHIER CLAUDE R'
S2         93   AU='AMICK B' OR AU='AMICK B W' OR AU='AMICK BRIAN W'
S3        185   S1 OR S2
S4         31   S3 AND IC=(G06F? OR G06G?)
File 347:JAPIO Nov 1976-2004/Feb(Updated 040607)
         (c) 2004 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2004/Jun W02
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040610,UT=20040603
         (c) 2004 WIPO/Univentio
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200437
         (c) 2004  Thomson Derwent
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4/5/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01656431
A METHOD AND SYSTEM FOR MONITORING AND PROFILING AN INTEGRATED CIRCUIT DIE TEMPERATURE
PROCEDE ET SYSTEME DE SURVEILLANCE ET DE PROFILAGE DE LA TEMPERATURE D'UN DE DE CIRCUIT INTEGRE
PATENT ASSIGNEE:
Sun Microsystems, Inc., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Applicant designated States: all)
INVENTOR:
GOLD, Spencer, M., 7 Ashley Street, Pepperell, MA 01463, (US)
GAUTHIER, Claude, R. , 405 Rancho Arroyo Parkway, 25, Fremont, CA 94536 , (US)
BOYLE, Steven, R., 1011 Lewis Street, Santa Clara, CA 95050, (US)
HOUSE, Kennth, A., 14 Beverly Road, Arlington, MA 02474, (US)
SIEGEL, Joseph, R., 11 Kalamat Circle, Shrewsbury, MA 01545, (US
PATENT (CC, No, Kind, Date): WO 2003077091 030918
APPLICATION (CC, No, Date): EP 2003744120 030219; WO 2003US5224 030219
PRIORITY (CC, No, Date): US 79476 020219
DESIGNATED STATES: AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES; FI; FR; GB; GR; HU; IE; IT; LI; LU; MC; NL
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO
INTERNATIONAL PATENT CLASS: **G06F-001/20**
LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 031112 A1 International application. (Art. 158(1))
Application: 031112 A1 International application entering European phase
LANGUAGE (Publication,Procedural,Application): English; English; English

4/5/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01592649
DESKEWING GLOBAL CLOCK SKEW USING LOCALIZED ADJUSTABLE DELAY CIRCUITS
REDRESSEMENT D'UN DESALIGNEMENT D'HORLOGE GLOBAL EFFECTUE A L'AIDE DE CIRCUITS A RETARD REGLABLES LOCALISES
PATENT ASSIGNEE:
Sun Microsystems, Inc., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Applicant designated States: all)
INVENTOR:
LIU, Dean, 1219 Crescent Terrace, Sunnyvale, CA 94086, (US)
THORP, Tyler, J., 473-H Costa Mesa Terrace, Sunnyvale, CA 94086, (US)
TRIVEDI, Pradeep, R., 992-6 Belmont Terrace, Sunnyvale, CA 94086, (US)
YEE, Gin, S., 171 Brahms Way, Sunnyvale, CA 94087, (US)
GAUTHIER, Claude, R. , 405 Rancho Arroyo Parkway, 25, Fremont, CA 94536 , (US
PATENT (CC, No, Kind, Date): WO 2003032137 030417
APPLICATION (CC, No, Date): EP 2002801041 021011; WO 2002US32578 021011
PRIORITY (CC, No, Date): US 975359 011011
DESIGNATED STATES: AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-001/10**
LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 030611 A2 International application. (Art. 158(1))
Application: 030611 A2 International application entering European phase
LANGUAGE (Publication,Procedural,Application): English; English; English

4/5/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01544858
METHOD FOR SMOOTHING DI/DT NOISE DUE TO CLOCK TRANSITIONS
VERFAHREN ZUR GLATTUNG VON DI/DT RAUSCH VERURSACHT DURCH TAKTUBERGANGE
PROCEDE PERMETTANT DE LISSER DU BRUIT DI/DT PROVOQUE PAR DES TRANSITIONS D'HORLOGE
PATENT ASSIGNEE:
Sun Microsystems, Inc., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Applicant designated States: all)
INVENTOR:
THORP, Tyler, J., 473-H Costa Mesa Terrace, Sunnyvale, CA 94086, (US)
AMICK, Brian, W. , 60 Babcock street #47, Brookline , MA 02446, (US)
LIU, Dean, 1219 Crescent Terrace, Sunnyvale, CA 94086, (US
LEGAL REPRESENTATIVE:
Weihs, Bruno (94362), Rosenthal & Osha, 121, avenue des Champs Elysees, 75008 Paris, (FR)
PATENT (CC, No, Kind, Date): EP 1425650 A2 040609 (Basic)
WO 2003001351 030103
APPLICATION (CC, No; Date): EP 2002737549 020620; WO 2002US19517 020620
PRIORITY (CC, No, Date): US 887395 010622
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-001/04** ; H03K-017/16; H03K-019/003
NOTE:
No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 030226 A2 International application. (Art. 158(1))
Application: 030226 A2 International application entering European phase
Application: 040609 A2 Published application without search report
Examination: 040609 A2 Date of request for examination: 20031217
LANGUAGE (Publication,Procedural,Application): English; English; English

4/5/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01511894
A LOW-COMPLEXITY, HIGH-ACCURACY MODEL OF A CPU POWER DISTRIBUTION SYSTEM
MODELL EINES CPU-ENERGIEVERTEILUNGSSYSTEMS MIT GERINGER KOMPLEXITAT UND HOHER GENAUIGKEIT
MODELE DE FAIBLE COMPLEXITE ET HAUTE PRECISION D'UN SYSTEME DE DISTRIBUTION ELECTRIQUE D'UC
PATENT ASSIGNEE:
Sun Microsystems, Inc., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Applicant designated States: all)
INVENTOR:
GAUTHIER, Claude, R. , 20207 Northbrook Sq., Cupertino, CA 95014, (US)
AMICK, Brian, W. , 60 Babcock Street#47, Brookline, MA 02446, (US
LEGAL REPRESENTATIVE:
Weihs, Bruno (94361), Rosenthal & Osha S.A.R.L. 121, avenue des Champs Elysees, 75008 Paris, (FR)
PATENT (CC, No, Kind, Date): EP 1379981 A2 040114 (Basic)
WO 2002080048 021010
APPLICATION (CC, No, Date): EP 2002719382 020328; WO 2002US9655 020328
PRIORITY (CC, No, Date): US 819773 010328
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-017/50**
NOTE:
No A-document published by EPO

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 021204 A2 International application. (Art. 158(1))
Application: 021204 A2 International application entering European phase
Application: 040114 A2 Published application without search report
Examination: 040114 A2 Date of request for examination: 20030926
Change: 040303 A2 Inventor information changed: 20040113
Change: 040414 A2 Inventor information changed: 20040225
LANGUAGE (Publication,Procedural,Application): English; English; English

4/5/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01511691
A LOW-COMPLEXITY, HIGH ACCURACY MODEL OF A CPU ANTI-RESONANCE SYSTEM
EIN MIT GERINGER KOMPLEXITAT, HOCHGENAUES MODELL EINES CPU-ANTIRESONANZSYSTEMS
MODELE DE SYSTEME D'ANTIRESONANCE D'UNITE CENTRALE (UC) TRES PRECIS, A FAIBLE COMPLEXITE
PATENT ASSIGNEE:
Sun Microsystems, Inc., (2616582), 901 San Antonio Road, M/S UPAL 01-521, Palo Alto, California 94303, (US), (Applicant designated States: all)
INVENTOR:
GAUTHIER, Claude, R. , 405 Rancho Arroyo Parkway 25, Fremont, CA 94536, (US)
AMICK, Brian, W. , 4600 Seton Center Parkway 309, Austin, TX 78759, (US
PATENT (CC, No, Kind, Date): WO 2002080047 021010
APPLICATION (CC, No, Date): EP 2002715223 020328; WO 2002US9606 020328
PRIORITY (CC, No, Date): US 819198 010328
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-017/50**
LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 021204 A2 International application. (Art. 158(1))
Application: 021204 A2 International application entering European phase
Application: 040526 A2 International application. (Art. 158(1))
Appl Changed: 040526 A2 International application not entering European phase
Withdrawal: 040526 A2 Date application deemed withdrawn: 20031029
LANGUAGE (Publication,Procedural,Application): English; English; English

4/5/6 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01047059 **Image available**
A METHOD AND SYSTEM FOR MONITORING AND PROFILING AN INTEGRATED CIRCUIT DIE TEMPERATURE
PROCEDE ET SYSTEME DE SURVEILLANCE ET DE PROFILAGE DE LA TEMPERATURE D'UN DE DE CIRCUIT INTEGRE
Patent Applicant/Assignee:
SUN MICROSYSTEMS INC, 4150 Network Circle, Santa Clara, CA 95054, US, US (Residence), US (Nationality)
Inventor(s):
GOLD Spencer M, 7 Ashley Street, Pepperell, MA 01463, US,
GAUTHIER Claude R , 405 Rancho Arroyo Parkway, #25, Fremont, CA 94536, US,
BOYLE Steven R, 1011 Lewis Street, Santa Clara, CA 95050, US,
HOUSE Kennth A, 14 Beverly Road, Arlington, MA 02474, US,
SIEGEL Joseph R, 11 Kalamat Circle, Shrewsbury, MA 01545, US
Legal Representative:

CANNING Kevin J (et al) (agent), Lahive & Cockfield, LLP, 28 State Street, Boston, MA 02109, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200377091 A1 20030918 (WO 0377091)
Application: WO 2003US5224 20030219 (PCT/WO US0305224)
Priority Application: US 200279476 20020219
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT SE SI SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-001/20**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 6107

English Abstract
A system and method are provided for sensing a physical stimulus of an integrated circuit. The system and method operate with one or more active thermal sensors embedded in the die of an integrated circuit to provide highly accurate die temperature measurements. The system and method are able to monitor and control the die temperature of the integrated circuit to avoid an integrated circuit malfunction due to an undesirable temperature condition.

French Abstract
L'invention porte sur un systeme et sur un procede de detection d'un stimulus physique d'un circuit integre. Ce systeme fonctionne avec au moins un capteur thermique actif encastre dans le de d'un circuit integre de facon a obtenir des mesures de temperature du de extrememement precises. Le systeme et le procede permettent de surveiller et commander la temperature du de du circuit integre pour eviter un dysfonctionnement dans le circuit integre imputable a une temperature non desiree.

Legal Status (Type, Date, Text)
Publication 20030918 A1 With international search report.
Examination 20031016 Request for preliminary examination prior to end of 19th month from priority date

4/5/7 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01002158 **Image available**
DESKEWING GLOBAL CLOCK SKEW USING LOCALIZED ADJUSTABLE DELAY CIRCUITS
REDRESSEMENT D'UN DESALIGNEMENT D'HORLOGE GLOBAL EFFECTUE A L'AIDE DE CIRCUITS A RETARD REGLABLES LOCALISES
Patent Applicant/Assignee:
SUN MICROSYSTEMS INC, 4150 Network Circle, Santa Clara, CA 95054, US, US (Residence), US (Nationality)
Inventor(s):
LIU Dean, 1219 Crescent Terrace, Sunnyvale, CA 94086, US,
THORP Tyler J, 473-H Costa Mesa Terrace, Sunnyvale, CA 94086, US,
TRIVEDI Pradeep R, 992-6 Belmont Terrace, Sunnyvale, CA 94086, US,
YEE Gin S, 171 Brahms Way, Sunnyvale, CA 94087, US,
GAUTHIER Claude R , 405 Rancho Arroyo Parkway, #25, Fremont, CA 94536, US
Legal Representative:
OSHA Jonathan (agent), Rosenthal & Osha L.L.P., 1221 McKinney, Suite

2800, Houston, TX 77010, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200332137 A2-A3 20030417 (WO 0332137)
Application: WO 2002US32578 20021011 (PCT/WO US0232578)
Priority Application: US 2001975359 20011011
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LU MC NL PT SE SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-001/10**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 2962

English Abstract
A method for reducing global clock skew by referencing a first point on an integrated circuit (80) to which to align other points on the integrated circuit (80) is provided. Further, an integrated circuit (80) that has localized adjustable delay circuits (84) having adjustable buffers (90) that selectively drive a signal on a clock grid (94) is provided. Further, a technique for using a local DLL (82), one or more phase detectors (86), and one or more adjustable delay circuits (84) connected to portions of a clock grid (94) to reduce clock skew is provided.

French Abstract
Cette invention concerne un procede permettant de reduire un desalignement d'horloge global selon lequel on reference un premier point sur un circuit integre sur lequel on aligne d'autres points sur le circuit integre. En outre, cette invention concerne un circuit integre comportant des circuits a retard reglables localises pourvus de tampons reglables qui entrainent de maniere selective un signal sur une grille d'horloge. De plus, cette invention concerne une technique consistant a utiliser une boucle a retard de phase (DLL) locale, un ou plusieurs detecteurs de phase et un ou plusieurs circuits a retard reglables connectes a des parties d'une grille d'horloge pour reduire un desalignement d'horloge.

Legal Status (Type, Date, Text)
Publication 20030417 A2 Without international search report and to be republished upon receipt of that report.
Examination 20030612 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20031211 Late publication of international search report
Republication 20031211 A3 With international search report.

4/5/8 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00971337 **Image available**
METHOD FOR SMOOTHING dI/dT NOISE DUE TO CLOCK TRANSITIONS
PROCEDE PERMETTANT DE LISSER DU BRUIT DI/DT PROVOQUE PAR DES TRANSITIONS D'HORLOGE
Patent Applicant/Assignee:
SUN MICROSYSTEMS INC, 4150 Network Circle, Santa Clara, CA 95054, US, US (Residence), US (Nationality)
Inventor(s):
THORP Tyler J, 473-H Costa Mesa Terrace, Sunnyvale, CA 94086, US,

AMICK Brian W , 4600 Seton Center Parkway, #309, Austin, TX 78759, US,
LIU Dean, 1219 Crescent Terrace, Sunnyvale, CA 94086, US
Legal Representative:
OSHA Jonathan P (et al) (agent), Rosenthal & Osha L.L.P., Suite 2800, 1221 McKinney, Houston, TX 77010, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200301351 A2-A3 20030103 (WO 0301351)
Application: WO 2002US19517 20020620 (PCT/WO US02019517)
Priority Application: US 2001887395 20010622
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-001/04**
International Patent Class: H03K-017/16; H03K-019/003
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 2395

English Abstract
A method for increasing a transition time period for an edge transition of a clock signal has been developed. The method includes detecting an edge transition of a clock signal of a computer system. Next, additional system power consumption is initiated upon detection of the edge transition. This additional power consumption will lengthen the edge transition time periode of the clock signal.
French Abstract
La presente invention concerne un procede permettant d'augmenter le delai de transition pour une transition de front d'un signal d'horloge. Ce procede consiste a detecter une transition de front du signal d'horloge d'un systeme informatique. Puis, a la detection de la transition de front, une consommation d'energie systeme supplementaire est declenchee. Cette consommation d'energie supplementaire permet d'allonger le delai de transition du signal d'horloge.

Legal Status (Type, Date, Text)
Publication 20030103 A2 Without international search report and to be republished upon receipt of that report.
Examination 20030220 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20040325 Late publication of international search report
Republication 20040325 A3 With international search report.

4/5/9 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00945878 **Image available**
A LOW-COMPLEXITY, HIGH-ACCURACY MODEL OF A CPU POWER DISTRIBUTION SYSTEM
MODELE DE FAIBLE COMPLEXITE ET HAUTE PRECISION D'UN SYSTEME DE DISTRIBUTION ELECTRIQUE D'UC
Patent Applicant/Assignee:
SUN MICROSYSTEMS INC, MS UPAL01-521, 901 San Antonio Road, Palo Alto, CA 94303, US, US (Residence), US (Nationality)
Inventor(s):
GAUTHIER Claude R , 405 Rancho Arroyo Parkway, #25, Fremont, CA 94536, US,
AMICK Brian W , 4600 Seton Center Parkway, #309, Austin, TX 78759, US
Legal Representative:

ROSENTHAL Alan D (et al) (agent), Rosenthal & Osha L.L.P., Suite 2800, 1221 McKinney, Houston, TX 77010, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200280048 A2-A3 20021010 (WO 0280048)
Application: WO 2002US9655 20020328 (PCT/WO US0209655)
Priority Application: US 2001819773 20010328
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-017/50**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 4406

English Abstract
A low-complexity, high accuracy model of a CPU power distribution system has been developed. The model includes models of multiple power converters that input to a board model. The board model then inputs to a package model. Finally, the package model inputs to a chip model. The model provides a high degree of accuracy with an acceptable simulation time.

French Abstract
Un modele de faible complexite et de haute precision d'un systeme de distribution electrique d'UC a ete developpe. Le modele contient des modeles de convertisseur de puissance multiples venant en entree dans un modele de carte. Le modele de carte entre alors dans un modele de boitier. Enfin, le modele de boitier entre dans un modele de puce. Le modele procure un degre eleve de precision avec un temps de simulation acceptable.

Legal Status (Type, Date, Text)
Publication 20021010 A2 Without international search report and to be republished upon receipt of that report.
Examination 20030206 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20030814 Late publication of international search report
Republication 20030814 A3 With international search report.

4/5/10 (Item 5 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00945877 **Image available**
A LOW-COMPLEXITY, HIGH ACCURACY MODEL OF A CPU ANTI-RESONANCE SYSTEM
MODELE DE SYSTEME D'ANTIRESONANCE D'UNITE CENTRALE (UC) TRES PRECIS, A FAIBLE COMPLEXITE
Patent Applicant/Assignee:
SUN MICROSYSTEMS INC, MS UPAL01-521, 901 San Antonio Road, Palo Alto, CA 94303, US, US (Residence), US (Nationality)
Inventor(s):
GAUTHIER Claude R , 405 Rancho Arroyo Parkway #25, Fremont, CA 94536, US ,
AMICK Brian W , 4600 Seton Center Parkway #309, Austin, TX 78759, US
Legal Representative:
ROSENTHAL Alan D (et al) (agent), Rosenthal & Osha L.L.P., Suite 2800, 1221 McKinney, Houston, TX 77010, US,
Patent and Priority Information (Country, Number, Date):

Patent: WO 200280047 A2-A3 20021010 (WO 0280047)
Application: WO 2002US9606 20020328 (PCT/WO US0209606)
Priority Application: US 2001819198 20010328
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-017/50**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 2883

English Abstract
A low-complexity, high accuracy model of a CPU anti-resonance system has been developed. The model includes a load model that simulates the performance of the anti-resonance circuit, a transistor that models the performance of a high frequency capacitor that models the performance of the intrinsic capacitance of a section of the microprocessor. All of the elements of the model are connected in parallel.

French Abstract
L'invention concerne le developpement d'un modele de systeme d'antiresonance UC tres precis, a faible complexite. Ce modele comporte un modele de charge qui simule la performance du circuit d'antiresonance, un transistor qui modelise la performance d'un condensateur haute frequence, et un condensateur qui modelise la performance de la capacitance intrinseque d'une section du microprocesseur. Tous les elements du modele sont connectes en parallele.

Legal Status (Type, Date, Text)
Publication 20021010 A2 Without international search report and to be republished upon receipt of that report.
Examination 20021205 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20031016 Late publication of international search report
Republication 20031016 A3 With international search report.
Republication 20031016 A3 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

4/5/11 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015962132 **Image available**
WPI Acc No: 2004-119973/200412
XRPX Acc No: N04-095906
Communication system identifies data signal bits that are not correctly latched, by comparing test pattern of latched data signal with preset pattern, after timing adjustment of copy of corresponding clock signal
Patent Assignee: AMICK B W (AMIC-I); GAUTHIER C R (GAUT-I); ROY A K (ROYA-I)
Inventor: **AMICK B W ; GAUTHIER C R ;** ROY A K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030233608	A1	20031218	US 2002174045	A	20020618	200412	B

Priority Applications (No Type Date): US 2002174045 A 20020618

Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 20030233608 A1   14 G01R-031/28

Abstract (Basic): US 20030233608 A1
NOVELTY - The communication links include data lines (414-428) and clock lines (416-430) for transmitting data and clock signals respectively. An adjustment circuit adjusts timing of a copy of clock signal relative to desired data signal, to determine when the data signal is to be latched. A comparator compares test pattern of latched signal to preset pattern, to identify signal bits that are not correctly latched.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for communication system updating method.
USE - Communication system.
ADVANTAGE - Enables identification and correction of improperly latched data signals bits, thereby ensuring data transmission with significantly reduced erroneous bits.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the communication system.
communication system (400)
communication circuits (412,434)
data lines (414-428)
clock lines (416-430)
control line (432)
pp; 14 DwgNo 4/7
Title Terms: COMMUNICATE; SYSTEM; IDENTIFY; DATA; SIGNAL; BIT; CORRECT; LATCH; COMPARE; TEST; PATTERN; LATCH; DATA; SIGNAL; PRESET; PATTERN; AFTER; TIME; ADJUST; COPY; CORRESPOND; CLOCK; SIGNAL
Derwent Class: S01; T01; U11
International Patent Class (Main): G01R-031/28
International Patent Class (Additional): **G06F-011/00**
File Segment: EPI

4/5/12 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015873689 **Image available**
WPI Acc No: 2004-031520/200403
XRPX Acc No: N04-024856
Loop bandwidth optimizing method for phase locked loop, involves adjusting loop bandwidth to control jitter that is estimated by simulating representative power supply waveform having noise
Patent Assignee: AMICK B (AMIC-I); GAUTHIER C (GAUT-I); LIU D (LIUD-I); TRIVEDI P (TRIV-I); SUN MICROSYSTEMS INC (SUNM)
Inventor: **AMICK B** ; **GAUTHIER C** ; LIU D; TRIVEDI P
Number of Countries: 001 Number of Patents: 002
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20030154453 A1 20030814 US 200275339 A 20020214 200403 B
US 6671863 B2 20031230 US 200275339 A 20020214 200406

Priority Applications (No Type Date): US 200275339 A 20020214
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 20030154453 A1   18 G06F-009/45
US 6671863 B2 G06F-009/45
Abstract (Basic): US 20030154453 A1
NOVELTY - A representative power supply waveform having noise obtained from a system including printed circuit board (PCB), is input into a simulation program of the phase locked loop (PLL) for estimating jitter of the PLL. The loop bandwidth of the PLL is adjusted until the jitter falls below a predetermined value.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) computer system for optimizing loop bandwidth in PLL; and
(2) computer-readable medium storing instructions for optimizing loop bandwidth.

USE - For optimizing loop bandwidth in phase locked loop (PLL) used with power supply network of computer system.

ADVANTAGE - Since representative power supply waveform having noise is used, an accurate circuit simulation requiring less computational load is performed.

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart explaining the loop bandwidth optimizing process.

pp; 18 DwgNo 6a/8

Title Terms: LOOP; BANDWIDTH; OPTIMUM; METHOD; PHASE; LOCK; LOOP; ADJUST; LOOP; BANDWIDTH; CONTROL; JITTER; ESTIMATE; SIMULATE; REPRESENT; POWER; SUPPLY; WAVEFORM; NOISE

Derwent Class: T01

International Patent Class (Main): **G06F-009/45**

International Patent Class (Additional): **G06F-017/50**

File Segment: EPI

4/5/13 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015873688 **Image available**

WPI Acc No: 2004-031519/200403

XRPX Acc No: N04-024855

Delay locked loop bandwidth optimization method in computer system, involves estimating jitter of loop based on input of power supply waveform with noise signal

Patent Assignee: AMICK B (AMIC-I); GAUTHIER C (GAUT-I); LIU D (LIUD-I); TRIVEDI P (TRIV-I); SUN MICROSYSTEMS INC (SUNM)

Inventor: **AMICK B** ; **GAUTHIER C** ; LIU D; TRIVEDI P

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030154447	A1	20030814	US 200275782	A	20020214	200403	B
US 6687881	B2	20040203	US 200275782	A	20020214	200413	

Priority Applications (No Type Date): US 200275782 A 20020214

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030154447	A1		17	G06F-017/50	
US 6687881	B2			G06F-017/50	

Abstract (Basic): US 20030154447 A1

NOVELTY - A power supply waveform with noise signal is input to simulate a delay locked loop (DLL). The jitter of DLL is estimated and correspondingly its loop bandwidth is adjusted. The process is repeated until the jitter falls below a predetermined amount.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) delay locked loop bandwidth optimization system; and
(2) computer readable medium storing delay locked loop bandwidth optimizing program.

USE - For optimizing delay locked loop bandwidth in computer system.

ADVANTAGE - Since power supply waveform having noise is used, an accurate circuit simulation is performed, thereby reducing the circuit design cost.

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart explaining the delay locked loop bandwidth optimizing process.

pp; 17 DwgNo 5a/7

Title Terms: DELAY; LOCK; LOOP; BANDWIDTH; OPTIMUM; METHOD; COMPUTER; SYSTEM; ESTIMATE; JITTER; LOOP; BASED; INPUT; POWER; SUPPLY; WAVEFORM; NOISE; SIGNAL

Derwent Class: T01

International Patent Class (Main): **G06F-017/50**

File Segment: EPI

4/5/14 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015851611 **Image available**
WPI Acc No: 2004-009438/200401
XRPX Acc No: N04-006711
Decoupling capacitance optimizing method for phase locked loops, involves estimating noise level in phase locked loop and adjusting decoupling capacitance until noise level falls below selected amount
Patent Assignee: AMICK B (AMIC-I); GAUTHIER C (GAUT-I); LIU D (LIUD-I); TRIVEDI P (TRIV-I)
Inventor: **AMICK B** ; **GAUTHIER C** ; LIU D; TRIVEDI P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030154064	A1	20030814	US 200275757	A	20020214	200401	B

Priority Applications (No Type Date): US 200275757 A 20020214
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030154064	A1		14	G06F-017/50	

Abstract (Basic): US 20030154064 A1
NOVELTY - The method involves inputting a representative power supply waveform with a noise to a simulation of a phase locked loop. The jitter level of the phase locked loop is estimated and an amount of decoupling capacitance is adjusted accordingly. The above steps are repeated until the jitter level falls below a selected amount.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) a system for optimizing decoupling capacitance in a phase locked loop
(b) a computer readable medium with recorded instructions for optimizing decoupling capacitance in a phase locked loop.
USE - Used for optimizing decoupling capacitance in phase locked loops.
ADVANTAGE - The waveform with noise avoids the over designing of the phase locked loop and decoupling capacitance with respect to control of noise, thereby reducing the simulation time. Hence the design of phase locked loop and the decoupling capacitance is modified in an iterative fashion resulting in improved system performance.
DESCRIPTION OF DRAWING(S) - The drawing shows a flow process of a decoupling capacitance optimizing method.
pp; 14 DwgNo 5/7
Title Terms: DECOUPLE; CAPACITANCE; OPTIMUM; METHOD; PHASE; LOCK; LOOP; ESTIMATE; NOISE; LEVEL; PHASE; LOCK; LOOP; ADJUST; DECOUPLE; CAPACITANCE; NOISE; LEVEL; FALL; BELOW; SELECT; AMOUNT
Derwent Class: T01; U23
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

4/5/15 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015835541 **Image available**
WPI Acc No: 2003-897745/200382
XRPX Acc No: N03-716483
Decoupling capacitance optimizing method for temperature sensor, involves determining difference between temperature representative input and output of sensor till difference falls below pre-selected value
Patent Assignee: AMICK B (AMIC-I); GAUTHIER C (GAUT-I); LIU D (LIUD-I);

TRIVEDI P (TRIV-I); SUN MICROSYSTEMS INC (SUNM)
Inventor: **AMICK B ; GAUTHIER C** ; LIU D; TRIVEDI P
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030154048	A1	20030814	US 200275205	A	20020214	200382	B
US 6704680	B2	20040309	US 200275205	A	20020214	200418	

Priority Applications (No Type Date): US 200275205 A 20020214
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030154048	A1		12	G01K-001/08	
US 6704680	B2			G05F-003/02	

Abstract (Basic): US 20030154048 A1

NOVELTY - The method involves inputting a representative power supply waveform having a noise to a stimulation of an on-chip temperature sensor. A difference between a temperature representative input and temperature dependent output of the sensor is determined. An amount of the decoupling capacitance is adjusted until the difference falls below a pre- selected value.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) a computer system

(b) a computer readable medium.

USE - Used for optimizing decoupling capacitance of on-chip temperature sensors.

ADVANTAGE - Since the power supply waveform having a noise is used, the on chip temperature sensor design and associated decoupling capacitor are not over designed with respect to temperature inaccuracy.

DESCRIPTION OF DRAWING(S) - The drawing shows a flow chart of the decoupling capacitance optimizing method.

pp; 12 DwgNo 3/5

Title Terms: DECOUPLE; CAPACITANCE; OPTIMUM; METHOD; TEMPERATURE; SENSE; DETERMINE; DIFFER; TEMPERATURE; REPRESENT; INPUT; OUTPUT; SENSE; TILL; DIFFER; FALL; BELOW; PRE; SELECT; VALUE
Derwent Class: S03; T01; U11
International Patent Class (Main): G01K-001/08; G05F-003/02
International Patent Class (Additional): G01R-031/02; **G06F-015/00** ; H01L-035/00
File Segment: EPI

4/5/16 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015767967 **Image available**
WPI Acc No: 2003-830169/200377
XRPX Acc No: N03-663284

Integrated circuit temperature monitoring system for microprocessor, includes controller which interprets asserted temperature value of thermal sensor, to monitor die temperature of circuit

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: BOYLE S R; **GAUTHIER C R** ; GOLD S M; HOUSE K A; SIEGEL J R; SIEGEL J
Number of Countries: 102 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030158697	A1	20030821	US 200279476	A	20020219	200377	B
WO 200377091	A1	20030918	WO 2003US5224	A	20030219	200377	
AU 2003216355	A1	20030922	AU 2003216355	A	20030219	200431	

Priority Applications (No Type Date): US 200279476 A 20020219
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030158697	A1		12	G01K-001/08	

WQ 200377091 A1 E G06F-001/20
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT SD SE SI SK SL SZ TR TZ UG ZM ZW
AU 2003216355 A1 G06F-001/20 Based on patent WO 200377091

Abstract (Basic): US 20030158697 A1
NOVELTY - Thermal sensors (14A-14C) measure temperature of integrated circuit (IC) (12) and asserts a value to represent the temperature. A controller (16) coupled to the thermal sensor, interprets asserted value to monitor the die temperature of integrated circuit. A calibration sensor (18) operates independent of the thermal sensors, to perform calibration temperature measurement.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(1) method for monitoring die temperature of integrated circuit; and
(2) temperature management system for integrated circuit.
USE - For very large-scale integration components such as microprocessor.
ADVANTAGE - The die temperature of the integrated circuit is monitored, controlled and calibrated to avoid malfunction caused by undesirable temperature conditions, by placing sensors at multiple die locations in circuit, to accurately track and monitor thermal gradient of circuit.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of integrated circuit with thermal sensor, calibration sensor and controller.
integrated circuit (12)
thermal sensors (14A-14C)
controller (16)
thermal calibration sensor (18)
microprocessor (24)
pp; 12 DwgNo 3/5
Title Terms: INTEGRATE; CIRCUIT; TEMPERATURE; MONITOR; SYSTEM; MICROPROCESSOR; CONTROL; INTERPRETATION; TEMPERATURE; VALUE; THERMAL; SENSE; MONITOR; DIE; TEMPERATURE; CIRCUIT
Derwent Class: S03; U11
International Patent Class (Main): G01K-001/08; **G06F-001/20**
International Patent Class (Additional): **G06F-015/00**
File Segment: EPI

4/5/17 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015767966 **Image available**
WPI Acc No: 2003-830168/200377
XRPX Acc No: N03-663283
Controller for monitoring temperature of integrated circuit, compares received measured temperature value with threshold, received through respective interfaces
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: **GAUTHIER C R** ; GOLD S; HOUSE K; ZARRINEH K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030158696	A1	20030821	US 200279475	A	20020219	200377	B

Priority Applications (No Type Date): US 200279475 A 20020219
Patent Details:

Patent No Kind Lan Pg   Main IPC   Filing Notes
US 20030158696 A1   13 G01K-001/08

Abstract (Basic): US 20030158696 A1
NOVELTY - A pair of interfaces (23,51) receive a value corresponding to measured temperature from a set of temperature sensors (14) and a value representing a threshold. A comparator compares the received value to check whether the measured values indicate the heating of integrated circuit (IC) (12).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for method for monitoring temperature of integrated circuit.
USE - For monitoring the temperature of integrated circuit (IC) e.g. very large-scale integration (VLSI), such as microprocessor.
ADVANTAGE - The effective temperature of integrated circuit is monitored, without any faults, for executing controls for preventing damage due to thermal problems.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram for the temperature monitoring controller of integrated circuit.
integrated circuit (12)
thermal sensor (14)
controller (16)
interfaces (23,51)
pp; 13 DwgNo 1A/5
Title Terms: CONTROL; MONITOR; TEMPERATURE; INTEGRATE; CIRCUIT; COMPARE; RECEIVE; MEASURE; TEMPERATURE; VALUE; THRESHOLD; RECEIVE; THROUGH; RESPECTIVE; INTERFACE
Derwent Class: S03; U11
International Patent Class (Main): G01K-001/08
International Patent Class (Additional): **G06F-015/00**
File Segment: EPI

4/5/18 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015693873 **Image available**
WPI Acc No: 2003-756062/200371
XRPX Acc No: N03-605856
On-chip temperature sensor accuracy estimation method involves inputting power supply waveform into simulation of on-chip temperature sensor and estimating accuracy of on-chip temperature sensor from simulation
Patent Assignee: AMICK B (AMIC-I); GAUTHIER C (GAUT-I); LIU D (LIUD-I); TRIVED P (TRIV-I); SUN MICROSYSTEMS INC (SUNM)
Inventor: **AMICK B** ; **GAUTHIER C** ; LIU D; TRIVED P; TRIVEDI P
Number of Countries: 001 Number of Patents: 002
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20030163277 A1 20030828 US 200275206 A 20020214 200371 B
US 6748339 B2 20040608 US 200275206 A 20020214 200437

Priority Applications (No Type Date): US 200275206 A 20020214
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 20030163277 A1   12 G06F-015/00
US 6748339 B2 G06F-015/00
Abstract (Basic): US 20030163277 A1
NOVELTY - A representative power supply waveform having noise is input into the simulation of on-chip temperature sensor. The accuracy of on-chip temperature sensor is estimated from the applied simulation.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(1) computer system for estimating accuracy of on-chip temperature sensor; and
(2) computer readable medium having instructions for estimating accuracy of on-chip temperature sensor.
USE - For estimating accuracy of on-chip temperature sensor mounted

on microprocessors such as CPU.

ADVANTAGE - More accurate simulation is performed with reduced cost and chip area when power supply waveform having noise is applied. The performance of CPU is improved.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the method of estimating accuracy of on-chip temperature sensor.

pp; 12 DwgNo 3a/5

Title Terms: CHIP; TEMPERATURE; SENSE; ACCURACY; ESTIMATE; METHOD; INPUT; POWER; SUPPLY; WAVEFORM; SIMULATE; CHIP; TEMPERATURE; SENSE; ESTIMATE; ACCURACY; CHIP; TEMPERATURE; SENSE; SIMULATE

Derwent Class: S03; T01

International Patent Class (Main): **G06F-015/00**

File Segment: EPI

4/5/19 (Item 9 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015693663 **Image available**

WPI Acc No: 2003-755852/200371

XRPX Acc No: N03-605667

Delay locked loop jitter estimating method, involves inputting representative power supply waveform having noise into simulation of locked loop to estimate jitter of locked loop

Patent Assignee: AMICK B (AMIC-I); GAUTHIER C (GAUT-I); LIU D (LIUD-I); TRIVEDI P (TRIV-I); SUN MICROSYSTEMS INC (SUNM)

Inventor: **AMICK B** ; **GAUTHIER C** ; LIU D; TRIVEDI P

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030154454	A1	20030814	US 200275320	A	20020214	200371	B
US 6691291	B2	20040210	US 200275320	A	20020214	200413	

Priority Applications (No Type Date): US 200275320 A 20020214

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030154454	A1		14	G06F-009/45	
US 6691291	B2			G06F-017/50	

Abstract (Basic): US 20030154454 A1

NOVELTY - The method involves inputting a representative power supply waveform having a noise into a simulation of a delayed locked loop (DLL) that comprises a processor and a memory. The power supply waveform and the simulation of the locked loop are obtained using simulation tools. A jitter of the locked loop is estimated from the simulation of the locked loop.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) a computer system for estimating jitter in a delay locked loop

(b) a computer readable medium for estimating jitter in a delay locked loop

USE - Used for estimating jitter in delay locked loop microprocessors.

ADVANTAGE - The power supply waveform is captured at a particular location in a network where the noise source is dominant, thereby performing accurate circuit simulation. The accurate power supply waveform results in a reduced chip area, thereby saving space for additional performance enhancing circuits. The DLL is more accurate because the digitized power supply waveform having noise is used instead of a sine or a square wave.

DESCRIPTION OF DRAWING(S) - The drawing shows a flow process of a delay locked loop (DLL) jitter estimation method.

pp; 14 DwgNo 3b/5

Title Terms: DELAY; LOCK; LOOP; JITTER; ESTIMATE; METHOD; INPUT; REPRESENT; POWER; SUPPLY; WAVEFORM; NOISE; SIMULATE; LOCK; LOOP; ESTIMATE; JITTER; LOCK; LOOP

Derwent Class: T01
International Patent Class (Main): **G06F-009/45 ; G06F-017/50**
International Patent Class (Additional): **G06F-017/50**
File Segment: EPI

4/5/20 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015693640 **Image available**
WPI Acc No: 2003-755829/200371
XRPX Acc No: N03-605644

Decoupling capacitance optimizing method for delay locked loops, involves estimating noise level in delay locked loop and adjusting decoupling capacitance until noise level falls below selected amount

Patent Assignee: AMICK B (AMIC-I); GAUTHIER C (GAUT-I); LIU D (LIUD-I); TRIVEDI P (TRIV-I)
Inventor: **AMICK B ; GAUTHIER C** ; LIU D; TRIVEDI P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030154065	A1	20030814	US 200275783	A	20020214	200371	B

Priority Applications (No Type Date): US 200275783 A 20020214
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030154065	A1		13	G06F-017/50	

Abstract (Basic): US 20030154065 A1

NOVELTY - The method involves inputting a representative power supply waveform with a noise to a simulation of a delay locked loop. The noise level of the delay locked loop is estimated and an amount of decoupling capacitance is adjusted accordingly. The above steps are repeated until the noise level falls below a selected amount.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) a system for optimizing decoupling capacitance in a delay locked loop

(b) a computer readable medium with recorded instructions for optimizing decoupling capacitance in a delay locked loop.

USE - Used for optimizing decoupling capacitance in delay locked loops.

ADVANTAGE - The waveform with noise avoids the over designing of the delay locked loop and decoupling capacitance with respect to control of noise, thereby reducing the simulation time. Hence the design of delay locked loop and the decoupling capacitance is modified in an iterative fashion resulting in improved microprocessor performance.

DESCRIPTION OF DRAWING(S) - The drawing shows a flow process of a decoupling capacitance optimizing method.

pp; 13 DwgNo 4/6

Title Terms: DECOUPLE; CAPACITANCE; OPTIMUM; METHOD; DELAY; LOCK; LOOP; ESTIMATE; NOISE; LEVEL; DELAY; LOCK; LOOP; ADJUST; DECOUPLE; CAPACITANCE; NOISE; LEVEL; FALL; BELOW; SELECT; AMOUNT
Derwent Class: T01; U23
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

4/5/21 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015668869 **Image available**
WPI Acc No: 2003-731056/200369
XRPX Acc No: N03-584375

Monolithic integrated circuit includes several thermal sensors which detect temperature of integrated circuit, and electrical fuse registers to store temperature calibration information of sensors

Patent Assignee: AMICK B (AMIC-I); GAUTHIER C (GAUT-I); GOLD S (GOLD-I); LIU D (LIUD-I); TRIVEDI P (TRIV-I); ZARRINEH K (ZARR-I)
Inventor: **AMICK B** ; **GAUTHIER C** ; GOLD S; LIU D; TRIVEDI P; ZARRINEH K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030158683	A1	20030821	US 200278760	A	20020219	200369	B

Priority Applications (No Type Date): US 200278760 A 20020219
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030158683	A1		11	G06F-019/00	

Abstract (Basic): US 20030158683 A1

NOVELTY - The monolithic integrated circuit (IC) includes several thermal sensors disposed on it, to detect the IC temperature. Several electrical fuse registers store the IC temperature calibration information of the thermal sensors.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) IC temperature calibration information storing method; and

(2) IC temperature determination method.

USE - Monolithic integrated circuit (IC).

ADVANTAGE - Since the IC temperature calibration information are stored in the electrical fuse registers of the IC, temperature of the IC is easily determined, by reading the stored information from the registers.

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart illustrating the IC temperature determination procedure.

pp; 11 DwgNo 5/5

Title Terms: MONOLITHIC; INTEGRATE; CIRCUIT; THERMAL; SENSE; DETECT; TEMPERATURE; INTEGRATE; CIRCUIT; ELECTRIC; FUSE; REGISTER; STORAGE; TEMPERATURE; CALIBRATE; INFORMATION; SENSE
Derwent Class: U11; U13
International Patent Class (Main): **G06F-019/00**
File Segment: EPI

4/5/22 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015608175 **Image available**
WPI Acc No: 2003-670332/200363
XRPX Acc No: N03-535183

Microprocessor power model simulation analysis method for designing microprocessor, involves generating summary information related to single cycle behavior of power data associated with specific cycles in power model simulation

Patent Assignee: AINGARAN K (AING-I); BLATT M G (BLAT-I); GAUTHIER C R (GAUT-I); GREENHILL D J (GREE-I)
Inventor: AINGARAN K; BLATT M G; **GAUTHIER C R** ; GREENHILL D J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030110019	A1	20030612	US 200110238	A	20011207	200363	B

Priority Applications (No Type Date): US 200110238 A 20011207
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030110019	A1		10	G06F-017/50	

Abstract (Basic): US 20030110019 A1

NOVELTY - The values of power data that are associated with the

specific simulation cycles are received from the power model simulator. The summary information relating to the single cycle behavior of the power data is generated, by calculating the peak single-cycle derivative of two particular power data of successive cycles . The power modeling simulation is analyzed using the generated summary information.

USE - For analyzing simulation results of microprocessor power model, for designing microprocessor.

ADVANTAGE - The summary information is gathered as file and stored in database, to help in the system cooling and charge pumps designing process and to avoid resonance frequencies. Helps in the design of microprocessor with minimum number and variety of charge pumps.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram explaining the summary information generation process.

pp; 10 DwgNo 3/5

Title Terms: MICROPROCESSOR; POWER; MODEL; SIMULATE; ANALYSE; METHOD; DESIGN; MICROPROCESSOR; GENERATE; SUMMARY; INFORMATION; RELATED; SINGLE; CYCLE; BEHAVE; POWER; DATA; ASSOCIATE; SPECIFIC; CYCLE; POWER; MODEL; SIMULATE

Derwent Class: T01; U11

International Patent Class (Main): **G06F-017/50**

File Segment: EPI

4/5/23 (Item 13 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015595866 **Image available**

WPI Acc No: 2003-658021/200362

XRPX Acc No: N03-524359

Input/output supply noise reducing method, involves connecting shunting device parallel with power supply of input/output supply that is activated and de-activated by external digital signal

Patent Assignee: AMICK B W (AMIC-I); GAUTHIER C R (GAUT-I); THORP T (THOR-I); SUN MICROSYSTEMS INC (SUNM)

Inventor: **AMICK B W** ; **GAUTHIER C R** ; THORP T

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030090310	A1	20030515	US 2001992607	A	20011114	200362	B
US 6701488	B2	20040302	US 2001992607	A	20011114	200417	

Priority Applications (No Type Date): US 2001992607 A 20011114

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030090310	A1		11	H03L-005/00	
US 6701488	B2			G06F-017/50	

Abstract (Basic): US 20030090310 A1

NOVELTY - The method involves supplying current to an input/output (I/O) supply (35) output from a power supply and connecting a shunting device (48) comprising an N-type transistor in parallel with the power supply of the I/O supply. The shunting device is selectively activated and deactivated independent of the I/O supply using an external digital signal.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for an apparatus for reducing noise in an I/O supply.

USE - Used for reducing noise of input/output supply in electronic circuits.

ADVANTAGE - The method provides low impedance current flow path and reduced voltage variation for an input/output supply system. Decreasing the noise in the I/O supply leads to increased predictability and less jitter on a signal transmitted by the I/O supply.

DESCRIPTION OF DRAWING(S) - The drawing shows a shunting resistance for reducing input/output supply noise.

Input/output supply (35)

Shunting device. (48)

pp; 11 DwgNo 5/8
Title Terms: INPUT; OUTPUT; SUPPLY; NOISE; REDUCE; METHOD; CONNECT; SHUNT; DEVICE; PARALLEL; POWER; SUPPLY; INPUT; OUTPUT; SUPPLY; ACTIVATE; DE; ACTIVATE; EXTERNAL; DIGITAL; SIGNAL
Derwent Class: U21; U24
International Patent Class (Main): **G06F-017/50** ; H03L-005/00
International Patent Class (Additional): H03K-005/08
File Segment: EPI

4/5/24 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015368950 **Image available**
WPI Acc No: 2003-429888/200340
XRPX Acc No: N03-343310

Voltage sensor for measuring voltage in IC, has VCO pulse counter whose output relative to expected count represents actual voltage at one section of IC

Patent Assignee: SUN MICROSYSTEMS INC (SUNM); AMICK B W (AMIC-I); GAUTHIER C R (GAUT-I)
Inventor: **AMICK B W** ; **GAUTHIER C R**
Number of Countries: 101 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030056124	A1	20030320	US 2001955681	A	20010919	200340	B
WO 200325598	A2	20030327	WO 2002US29570	A	20020918	200340	
GB 2395020	A	20040512	WO 2002US29570	A	20020918	200432	
			GB 20044441	A	20040227		

Priority Applications (No Type Date): US 2001955681 A 20010919
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030056124	A1		7	G06F-001/26	
WO 200325598	A2	E		G01R-031/27	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW

GB 2395020	A			G01R-031/27	Based on patent WO 200325598

Abstract (Basic): US 20030056124 A1

NOVELTY - The voltage sensor (10) has a VCO (voltage controlled oscillator) pulse counter (14) and a clock pulse counter (18) disposed in an IC to count the number of pulses generated by a VCO (12) and the number of pulses on a clock signal, respectively. The result of the VCO pulse counter relative to an expected count represents the actual voltage at a section of the IC.

DETAILED DESCRIPTION - The VCO is also disposed in the IC.

INDEPENDENT CLAIMS are included for the following:

(a) the use method of the voltage sensor for measuring voltage at a section of an IC; and

(b) the IC.

USE - For measuring voltage in a section in an IC.

ADVANTAGE - Provides useful parameters for helping chip designers understand and improve chip behavior. Can be used on-chip for accurately determining the voltage at a section of a computer chip. Increases chip performance and efficiency. Improves power grid integrity through design.

DESCRIPTION OF DRAWING(S) - The figure shows a circuit diagram of the ON-chip voltage sensor.

Voltage sensor (10)

VCO (12)

VCO pulse counter (14)
Clock pulse counter (18)
pp; 7 DwgNo 1/3
Title Terms: VOLTAGE; SENSE; MEASURE; VOLTAGE; IC; VCO; PULSE; COUNTER; OUTPUT; RELATIVE; COUNT; REPRESENT; ACTUAL; VOLTAGE; ONE; SECTION; IC
Derwent Class: U13; U21; U22
International Patent Class (Main): G01R-031/27; **G06F-001/26**
International Patent Class (Additional): G01R-019/252; **G06F-001/28** ; **G06F-001/30**
File Segment: EPI

4/5/25 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015302487 **Image available**
WPI Acc No: 2003-363421/200334
XRPX Acc No: N03-290216

Integrated circuit to reduce global clock skew in e.g. computer system that includes localized adjustable delay circuits with adjustable buffers

Patent Assignee: GAUTHIER C R (GAUT-I); LIU D (LIUD-I); THORP T J (THOR-I); TRIVEDI P R (TRIV-I); YEE G S (YEEG-I); SUN MICROSYSTEMS INC (SUNM)
Inventor: **GAUTHIER C R** ; LIU D; THORP T J; TRIVEDI P R; YEE G S
Number of Countries: 101 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200332137	A2	20030417	WO 2002US32578	A	20021011	200334	B
US 20030071669	A1	20030417	US 2001975359	A	20011011	200340	
US 6686785	B2	20040203	US 2001975359	A	20011011	200413	

Priority Applications (No Type Date): US 2001975359 A 20011011
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200332137	A2	E	16	G06F-001/10	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW

US 20030071669	A1		H03L-007/06
US 6686785	B2		H03L-007/06

Abstract (Basic): WO 200332137 A2
NOVELTY - Includes localized adjustable delay circuits with adjustable buffers. A first point on the integrated circuit is referenced and other points on the integrated circuit are aligned with respect to this point. The delay circutis then selectively drive a signal on a clock grid.
DETAILED DESCRIPTION - A local DLL, several phase detectors, and several adjustable delay circuits connected to parts of a clock grid can be used to reduce clock skew. An INDEPENDENT CLAIM is included for a method.
USE - For reducing global clock skew in e.g. computer system.
ADVANTAGE - Accounts for clock skew introduced by devices and variations in the local distribution layer.
DESCRIPTION OF DRAWING(S) - The drawing shows the component layout of the circuit.
pp; 16 DwgNo 4a/5
Title Terms: INTEGRATE; CIRCUIT; REDUCE; GLOBE; CLOCK; SKEW; COMPUTER; SYSTEM; LOCALISE; ADJUST; DELAY; CIRCUIT; ADJUST; BUFFER
Derwent Class: T01
International Patent Class (Main): **G06F-001/10** ; H03L-007/06
File Segment: EPI

4/5/26 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015251623 **Image available**
WPI Acc No: 2003-312549/200330
Related WPI Acc No: 2003-392503
XRPX Acc No: N03-248957

Current change rate magnitude reducing method for integrated circuit, involves gradually reducing amount of current sourced by power supply based on determination

Patent Assignee: SUN MICROSYSTEMS INC (SUNM); AMICK B W (AMIC-I); GAUTHIER C R (GAUT-I); THORP T J (THOR-I); WHEELER R L (WHEE-I)
Inventor: **AMICK B W ; GAUTHIER C R ;** THORP T J; WHEELER R L
Number of Countries: 101 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030037267	A1	20030220	US 2001930373	A	20010814	200330	B
WO 200317490	A1	20030227	WO 2002US25849	A	20020814	200330	
EP 1421691	A1	20040526	EP 2002761371	A	20020814	200435	
			WO 2002US25849	A	20020814		

Priority Applications (No Type Date): US 2001930373 A 20010814; US 2001930030 A 20010814
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030037267	A1		6	G06F-001/26	
WO 200317490	A1	E		H03K-017/16	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW

EP 1421691	A1	E		H03K-017/16	Based on patent WO 200317490

Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

Abstract (Basic): US 20030037267 A1

NOVELTY - An amount of current sourced by power supply, is reduced gradually based on a determination of a time at which the power consumption by a integrated circuit (IC) needs to be reduced.

USE - For reducing magnitude of rate of current change of IC e.g. microprocessor.

ADVANTAGE - Enables the microprocessor to run with less noise, since several transistors are used to reduce the power consumption. Enables the microprocessor to operate quickly. Reduces the chance of power supply damage, and reduces the effect on average power consumption, since the magnitude of rate of the current change is reduced gradually.

DESCRIPTION OF DRAWING(S) - The figure shows a circuit diagram explaining the current change rate magnitude reducing method.

pp; 6 DwgNo 2a/2

Title Terms: CURRENT; CHANGE; RATE; MAGNITUDE; REDUCE; METHOD; INTEGRATE; CIRCUIT; GRADUAL; REDUCE; AMOUNT; CURRENT; POWER; SUPPLY; BASED; DETERMINE
Derwent Class: T01; U13; U21; U24
International Patent Class (Main): **G06F-001/26** ; H03K-017/16
File Segment: EPI

4/5/27 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015033528 **Image available**
WPI Acc No: 2003-094045/200308
XRPX Acc No: N03-074485

Method of reducing noise due to clock transitions in microelectronic circuitry, initiates additional system power consumption on detecting the edge transitions of the clock signal

Patent Assignee: AMICK B W (AMIC-I); LIU D (LIUD-I); THORP T J (THOR-I); SUN MICROSYSTEMS INC (SUNM)
Inventor: **AMICK B W** ; LIU D; THORP T J
Number of Countries: 100 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200301351	A2	20030103	WO 2002US19517	A	20020620	200308	B
US 6515527	B2	20030204	US 2001887395	A	20010622	200313	
US 20020196075	A1	20021226	US 2001887395	A	20010622	200315	

Priority Applications (No Type Date): US 2001887395 A 20010622
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200301351	A2	E	12	G06F-001/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

US 6515527	B2		H03K-005/12
US 20020196075	A1		H03B-001/00

Abstract (Basic): WO 2003001351 A2

NOVELTY - The method of reducing noise detects an edge transition (44,45) of the clock signal (40) and initiates additional system power consumption in response to the transition, effectively lengthening the transition time (48) of the clock signal edges.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for an apparatus for increasing a transition time period for an edge transition of a clock signal.

USE - For use in microelectronic circuitry.

ADVANTAGE - Initiating additional system power on detecting edge transitions of the clock signal, lengthens the edge transition time, thus reducing noise due to instantaneous current demand during clock transitions.

DESCRIPTION OF DRAWING(S) - The figure shows a graph of a clock signal.

Clock signal (40)
Edge transitions of the clock signal (44, 45)
Time period of the edge transition (48)
pp; 12 DwgNo 4/5

Title Terms: METHOD; REDUCE; NOISE; CLOCK; TRANSITION; MICROELECTRONIC; CIRCUIT; INITIATE; ADD; SYSTEM; POWER; CONSUME; DETECT; EDGE; TRANSITION; CLOCK; SIGNAL
Derwent Class: T01; U13; U22
International Patent Class (Main): **G06F-001/00** ; H03B-001/00; H03K-005/12
File Segment: EPI

4/5/28 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015030827 **Image available**
WPI Acc No: 2003-091344/200308
XRPX Acc No: N03-072279

CPU power system modeling apparatus for computer system, has multiple DC/DC power converter models that input to board model which then inputs to package model

Patent Assignee: SUN MICROSYSTEMS INC (SUNM); AMICK B W (AMIC-I);
GAUTHIER C R (GAUT-I)
Inventor: **AMICK B W ; GAUTHIER C R**
Number of Countries: 101 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020143514	A1	20021003	US 2001819773	A	20010328	200308	B
WO 200280048	A2	20021010	WO 2002US9655	A	20020328	200308	
EP 1379981	A2	20040114	EP 2002719382	A	20020328	200410	
			WO 2002US9655	A	20020328		
AU 2002250470	A1	20021015	AU 2002250470	A	20020328	200432	

Priority Applications (No Type Date): US 2001819773 A 20010328
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020143514	A1		12	G06F-017/50	
WO 200280048	A2	E		G06F-017/50	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

EP 1379981	A2	E	G06F-017/50	Based on patent WO 200280048

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

AU 2002250470	A1		G06F-017/50	Based on patent WO 200280048

Abstract (Basic): US 20020143514 A1
NOVELTY - Multiple DC/DC power converter models input to a board model which then inputs to a package model. The package model inputs to a chip model which comprises bump and grid models, load models and channel modes.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for method for modeling a power system.
USE - For modeling CPU power system of a computer system.
ADVANTAGE - Provides high degree of accuracy with an acceptable simulation time and low complexity.
DESCRIPTION OF DRAWING(S) - The figure shows the circuit model of a board.
pp; 12 DwgNo 4/9
Title Terms: CPU; POWER; SYSTEM; APPARATUS; COMPUTER; SYSTEM; MULTIPLE; DC; DC; POWER; CONVERTER; MODEL; INPUT; BOARD; MODEL; INPUT; PACKAGE; MODEL
Derwent Class: T01; U24
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

4/5/29 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014997524 **Image available**
WPI Acc No: 2003-058039/200305
XRPX Acc No: N03-045055
Anti-resonance circuit modeling apparatus used in computer, has transistor and capacitor connected in parallel with load model to simulate high frequency capacitor and microprocessor intrinsic capacitance
Patent Assignee: SUN MICROSYSTEMS INC (SUNM); AMICK B W (AMIC-I);
GAUTHIER C R (GAUT-I)
Inventor: **AMICK B W ; GAUTHIER C R**
Number of Countries: 100 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020143509	A1	20021003	US 2001819198	A	20010328	200305	B

WQ 200280047 A2 20021010 WO 2002US9606 A 20020328 200305
AU 2002247434 A1 20021015 AU 2002247434 A 20020328 200432

Priority Applications (No Type Date): US 2001819198 A 20010328
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20020143509 A1 10 G06F-017/50
WO 200280047 A2 E G06F-017/50
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW
AU 2002247434 A1 G06F-017/50 Based on patent WO 200280047

Abstract (Basic): US 20020143509 A1
NOVELTY - The modeling apparatus has a transistor connected in parallel with a load model that simulates the anti-resonance circuit with a voltage controlled resistor, to simulate a high frequency capacitor. A capacitor connected in parallel with the load model simulates an intrinsic capacitance of a microprocessor.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for anti-resonance circuit modeling method.
USE - For modeling anti-resonance circuit of microprocessor such as central processing unit (CPU) used in computers.
ADVANTAGE - The modeling of anti-resonance circuits of microprocessor chips is performed by a low complexity with an excellent simulation time. The model also provides flexibility in accurately modeling the system performance.
DESCRIPTION OF DRAWING(S) - The figure shows a graph of the oscillating circuit.
pp; 10 DwgNo 2/10
Title Terms: ANTI; RESONANCE; CIRCUIT; APPARATUS; COMPUTER; TRANSISTOR; CAPACITOR; CONNECT; PARALLEL; LOAD; MODEL; SIMULATE; HIGH; FREQUENCY; CAPACITOR; MICROPROCESSOR; INTRINSIC; CAPACITANCE
Derwent Class: T01
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

4/5/30 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014705612 **Image available**
WPI Acc No: 2002-526316/200256
XRPX Acc No: N02-416489
Digital signal pre-emphasizing method involves using predriver for pre-emphasizing transition in value between input data bit and previous data bit
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: **GAUTHIER C R**
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 6392443 B1 20020521 US 2000504508 A 20000215 200256 B

Priority Applications (No Type Date): US 2000504508 A 20000215
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 6392443 B1 8 H03K-019/94

Abstract (Basic): US 6392443 B1
NOVELTY - The data bit (46) is received as input for the flip-flop (44a). The data bit and its complement is output from the flip flop to

another flip flop (44b). The previous and the output data bits and their complements are received and input to a predriver. A transition in value between the data bit and the previous data bit is pre-emphasized by the predriver.

USE - For pre-emphasizing high frequency digital signal in application specific integrated circuit (ASIC) implementations.

ADVANTAGE - A single drive stage is needed for pre-emphasizing a high frequency signal. This allows for a reduction of power dissipation, a reduction in required area on the chip and an increase in the bandwidth.

DESCRIPTION OF DRAWING(S) - The figure shows an N-channel implementation of pre-emphasis circuit.

Flip flop (44a,44b)

Data bit (46)

pp; 8 DwgNo 5/9

Title Terms: DIGITAL; SIGNAL; PRE; EMPHASIS; METHOD; PRE; EMPHASIS; TRANSITION; VALUE; INPUT; DATA; BIT; DATA; BIT

Derwent Class: U13; U22

International Patent Class (Main): H03K-019/94

International Patent Class (Additional): **G06G-007/16**

File Segment: EPI

4/5/31 (Item 21 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014621934 **Image available**

WPI Acc No: 2002-442638/200247

XRPX Acc No: N02-348629

Pre-emphasizing circuit for digital signal, has pre-driver for pre-emphasizing transition between two consecutive data bits to output equalized digital signal

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)

Inventor: **GAUTHIER C R**

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6377076	B1	20020423	US 2000503144	A	20000215	200247	B

Priority Applications (No Type Date): US 2000503144 A 20000215

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6377076	B1		9	H03K-019/0175	

Abstract (Basic): US 6377076 B1

NOVELTY - A pre-driver circuit (64) receives input data bit and its complement and the previous data bit and its complement, and pre-emphasizes a transition in value between the two consecutive data bits and outputs an equalized digital signal.

USE - For high-frequency pre-emphasis of digital signal in digital system for application specific integrated circuit (ASIC) implementations.

ADVANTAGE - Increases signal to noise ratio significantly and consequently reduces deterministic filter. Only a single driver stage is used for pre-emphasizing a high frequency signal which allows for reduction of power-dissipation, a reduction is required area on the chip and on increase in the bandwidth.

DESCRIPTION OF DRAWING(S) - The figure shows an N-channel implementation of a pre-emphasis circuit.

Pre-driver (64)

pp; 9 DwgNo 5/9

Title Terms: PRE; EMPHASIS; CIRCUIT; DIGITAL; SIGNAL; PRE; DRIVE; PRE; EMPHASIS; TRANSITION; TWO; CONSECUTIVE; DATA; BIT; OUTPUT; DIGITAL; SIGNAL

Derwent Class: T02; U21

International Patent Class (Main): H03K-019/0175

International Patent Class (Additional): **G06G-007/16** ; H03K-019/094
File Segment: EPI

```
Set     Items   Description
S1       1002   AU=(GAUTHIER, C? OR GAUTHIER C? OR AMICK, B? OR AMICK B?)
S2          0   S1 AND POWER()CONVERTER()MODEL?
File   2:INSPEC 1969-2004/Jun W1
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Jun W2
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2004/Jun W1
         (c) 2004 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Jun W2
         (c) 2004 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Jun W2
         (c) 2004 BLDSC all rts. reserv.
File  92:IHS Intl.Stds.& Specs. 1999/Nov
         (c) 1999 Information Handling Services
File  94:JICST-EPlus 1985-2004/May W4
         (c)2004 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2004/May W5
         (c) 2004 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/May
         (c) 2004 The HW Wilson Co.
File 103:Energy SciTec 1974-2004/Jun B1
         (c) 2004 Contains copyrighted material
File 144:Pascal 1973-2004/Jun W1
         (c) 2004 INIST/CNRS
File 202:Info. Sci. & Tech. Abs. 1966-2004/May 14
         (c) 2004 EBSCO Publishing
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File 239:Mathsci 1940-2004/Aug
         (c) 2004 American Mathematical Society
File 275:Gale Group Computer DB(TM) 1983-2004/Jun 18
         (c) 2004 The Gale Group
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 647:CMP  Computer Fulltext 1988-2004/Jun W1
         (c) 2004 CMP Media, LLC
File 674:Computer News Fulltext 1989-2004/Jun W2
         (c) 2004 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2004/Jun 17
         (c) 2004 The Dialog Corp.
```

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Set     Items   Description
S1    2257222   MODEL? ? OR VISUAL? OR DIAGRAM? OR GRAPHIC? OR DISPLAY? OR
            CHART? OR REPRESENT? OR GRAPH? ?
S2          2   POWER()CONVERTER()S1
S3    2413307   PLURAL? OR VARIOUS OR SEVERAL OR MULTIPL? OR MANY OR NUMER-
            OUS OR UNLIMITED
S4       2378   (BOARD OR CONTROLLER)()S1
S5        159   PACKAGE? () S1
S6        879   (CHIP? ? OR MICROCHIP OR INTEGRATED()CIRCUIT? OR IC OR RAM
            OR RANDOM()ACCESS()MEMORY OR DRAM? OR SRAM? OR ROM? OR PROM? -
            OR EPROM? OR EEPROM? OR FLASH)()S1
S7    8223035   COMPRIS? OR INCLUDE? OR CONTAIN?
S8          0   (BUMP AND GRIND)()S1
S9        423   LOAD()S1
S10       693   CHANNEL()S1
S11    236182   (DC OR DIRECT()CURRENT) AND (DC OR DIRECT()CURRENT)
S12       102   VOLTAGE()CONTROL?()RESISTOR?
S13     37038   CURRENT()SOURCE?
S14        12   (INTERCONNECTING OR INTER()CONNECTING)()GRID?
S15         1   THREE()SECTION()GRID
S16         4   (BUMP OR GRIND)()S1
S17         1   S2 AND S4 AND S5
S18         2   S5 AND S6
S19         0   S6 AND S7 AND S16
S20         0   S6 AND S16
S21         0   S6 AND S9 AND S10
S22         1   S6 AND S9
S23         0   S6 AND S10
S24         1   S6 AND CHANNEL()MODE?
S25         1   S9 AND S12
S26         2   S9 AND S13
S27      2156   SECTION()S1
S28         0   S27 AND S14
S29         0   S27 AND S15
S30        23   S2 OR S14 OR S15 OR S16 OR S17 OR S18 OR S22 OR S24 OR S25
            OR S26
S31         4   S30 AND IC=(G06F? OR G06G?)
S32         1   S30 AND MC=(T01-J15A4 OR T01-L01 OR U24-D01X OR U24-D02)
S33         4   S31 OR S32
File 347:JAPIO Nov 1976-2004/Feb(Updated 040607)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200437
         (c) 2004  Thomson Derwent
```

33/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03442667 **Image available**
CIRCUIT SIMULATION METHOD

PUB. NO.: 03-105567 [JP 3105567 A]
PUBLISHED: May 02, 1991 (19910502)
INVENTOR(s): NIIMI TOSHIO
IHIRA SUSUMU
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-241992 [JP 89241992]
FILED: September 20, 1989 (19890920)
INTL CLASS: [5] **G06F-015/60**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 1233, Vol. 15, No. 301, Pg. 79, July 31, 1991 (19910731)

ABSTRACT

PURPOSE: To shorten the calculation processing time of a joint part together with improvement of accuracy by transmitting the voltage and the current to a part of a nodal point where the signals are outputted via a 1st connection circuit and to a part of a nodal point where the signals are inputted via a 2nd connection circuit respectively.

CONSTITUTION: A **load model** of parallel connection consisting of a resistance, a **current source** , and a capacity is connected between the ground and a nodal point 1 where the signals are transmitted to a digital part from an analog part. At the same time, a model of parallel connection consisting of a **current source** and a resistance is inserted between the ground and a nodal point 2 where the signals are transmitted to the analog part from the digital part. In other words, an entire analog-digital circuit is divided into pieces and the signals are transmitted to the digital part from the digital part from the analog part via a connection circuit 1 and vice versa via a connection circuit 2 respectively. Thus the circuits of the analog and digital parts can be analyzed independently of each other. As a result, the model calculating time is shortened together with reduction of the circuit scale. Furthermore the voltage-to- current dependence between the input and output sides of the digital part can be shown with high accuracy via the connection circuit.

33/5/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015030827 **Image available**
WPI Acc No: 2003-091344/200308
XRPX Acc No: N03-072279
CPU power system modeling apparatus for computer system, has multiple DC/DC power converter models **that input to** board model **which then inputs to** package model
Patent Assignee: SUN MICROSYSTEMS INC (SUNM); AMICK B W (AMIC-I); GAUTHIER C R (GAUT-I)
Inventor: AMICK B W; GAUTHIER C R
Number of Countries: 101 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020143514	A1	20021003	US 2001819773	A	20010328	200308 B
WO 200280048	A2	20021010	WO 2002US9655	A	20020328	200308
EP 1379981	A2	20040114	EP 2002719382	A	20020328	200410
			WO 2002US9655	A	20020328	
AU 2002250470	A1	20021015	AU 2002250470	A	20020328	200432

Priority Applications (No Type Date): US 2001819773 A 20010328

Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20020143514 A1 12 G06F-017/50
WO 200280048 A2 E G06F-017/50
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW
EP 1379981 A2 E G06F-017/50 Based on patent WO 200280048
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
AU 2002250470 A1 G06F-017/50 Based on patent WO 200280048

Abstract (Basic): US 20020143514 A1
NOVELTY - Multiple DC/DC **power converter models** input to a **board model** which then inputs to a **package model** . The **package model** inputs to a **chip model** which comprises bump and grid models, **load models** and **channel modes** .
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for method for modeling a power system.
USE - For modeling CPU power system of a computer system.
ADVANTAGE - Provides high degree of accuracy with an acceptable simulation time and low complexity.
DESCRIPTION OF DRAWING(S) - The figure shows the circuit model of a board.
pp; 12 DwgNo 4/9
Title Terms: CPU; POWER; SYSTEM; APPARATUS; COMPUTER; SYSTEM; MULTIPLE; DC; DC; POWER; CONVERTER; MODEL; INPUT; BOARD; MODEL; INPUT; PACKAGE; MODEL
Derwent Class: T01; U24
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

33/5/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014997524 **Image available**
WPI Acc No: 2003-058039/200305
XRPX Acc No: N03-045055
Anti-resonance circuit modeling apparatus used in computer, has transistor and capacitor connected in parallel with load model **to simulate high frequency capacitor and microprocessor intrinsic capacitance**
Patent Assignee: SUN MICROSYSTEMS INC (SUNM); AMICK B W (AMIC-I); GAUTHIER C R (GAUT-I)
Inventor: AMICK B W; GAUTHIER C R
Number of Countries: 100 Number of Patents: 003
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20020143509 A1 20021003 US 2001819198 A 20010328 200305 B
WO 200280047 A2 20021010 WO 2002US9606 A 20020328 200305
AU 2002247434 A1 20021015 AU 2002247434 A 20020328 200432

Priority Applications (No Type Date): US 2001819198 A 20010328
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20020143509 A1 10 G06F-017/50
WO 200280047 A2 E G06F-017/50
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW
AU 2002247434 A1 G06F-017/50 Based on patent WO 200280047

Abstract (Basic): US 20020143509 A1

NOVELTY - The modeling apparatus has a transistor connected in parallel with a **load model** that simulates the anti-resonance circuit with a **voltage controlled resistor** , to simulate a high frequency capacitor. A capacitor connected in parallel with the **load model** simulates an intrinsic capacitance of a microprocessor.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for anti-resonance circuit modeling method.

USE - For modeling anti-resonance circuit of microprocessor such as central processing unit (CPU) used in computers.

ADVANTAGE - The modeling of anti-resonance circuits of microprocessor chips is performed by a low complexity with an excellent simulation time. The model also provides flexibility in accurately modeling the system performance.

DESCRIPTION OF DRAWING(S) - The figure shows a graph of the oscillating circuit.

pp; 10 DwgNo 2/10

Title Terms: ANTI; RESONANCE; CIRCUIT; APPARATUS; COMPUTER; TRANSISTOR; CAPACITOR; CONNECT; PARALLEL; LOAD; MODEL; SIMULATE; HIGH; FREQUENCY; CAPACITOR; MICROPROCESSOR; INTRINSIC; CAPACITANCE
Derwent Class: T01
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

33/5/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004364506
WPI Acc No: 1985-191384/198532
XRPX Acc No: N85-143617

Integrated circuit connection matrix for wafer substrate - enables faulty circuits isolated by fuses to be replaced by operating circuits

Patent Assignee: INOVA MICROELTRN (INOV-N); VARSHNEY R C (VARS-I)
Inventor: VARSHNEY R C
Number of Countries: 006 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3503433	A	19850801	DE 3503433	A	19850201	198532	B
GB 2153590	A	19850821	GB 852400	A	19850131	198534	
FR 2558989	A	19850802				198537	
JP 60182151	A	19850917	JP 8516706	A	19850201	198543	
US 4703436	A	19871027	US 84576066	A	19840201	198745	
GB 2153590	B	19871216	GB 852404	A	19850131	198750	
CA 1236918	A	19880517				198824	

Priority Applications (No Type Date): US 84576066 A 19840201
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3503433	A		62		

Abstract (Basic): DE 3503433 A

A connecting matrix is used to obtain a permissible distribution of fully operating, partly operating and non-operating integrated circuits on a wafer. Each circuit is tested separately and a conductive grid is formed on the wafer for forming connections. The non operating circuits determined before adding the grid are separated from the grid by fuse elements.

Each line of the matrix contains redundant decoding lines, so that a computer controlled program can be used to reallocate operative circuits to other zones containing defective circuits, to obtain completely operating matrix lines. They are interconnected with input

and output lines with bit positions within input and output bytes.

USE/ADVANTAGE - Suitable multiple circuit structures can be readily built up.

/11

Title Terms: INTEGRATE; CIRCUIT; CONNECT; MATRIX; WAFER; SUBSTRATE; ENABLE; FAULT; CIRCUIT; ISOLATE; FUSE; REPLACE; OPERATE; CIRCUIT

Derwent Class: U11; U13; U14

International Patent Class (Additional): G01R-031/28; **G06F-015/60** ; G11C-005/02; G11C-007/00; G11C-008/00; G11C-011/34; H01L-021/88; H01L-023/52; H01L-027/10

File Segment: EPI

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Set     Items   Description
S1      37638   MODEL? ? OR VISUAL? OR DIAGRAM? OR GRAPHIC? OR DISPLAY? OR
             CHART? OR REPRESENT? OR GRAPH? ?
S2          0   POWER()CONVERTER()S1
S3      46505   PLURAL? OR VARIOUS OR SEVERAL OR MULTIPL? OR MANY OR NUMER-
             OUS OR UNLIMITED
S4          5   (BOARD OR CONTROLLER)()S1
S5         55   PACKAGE? () S1
S6        111   (CHIP? ? OR MICROCHIP OR INTEGRATED()CIRCUIT? OR IC OR RAM
             OR RANDOM()ACCESS()MEMORY OR DRAM? OR SRAM? OR ROM? OR PROM? -
             OR EPROM? OR EEPROM? OR FLASH)()S1
S7      41605   COMPRIS? OR INCLUDE? OR CONTAIN?
S8          0   (BUMP AND GRIND)()S1
S9          6   LOAD()S1
S10         9   CHANNEL()S1
S11        84   (DC OR DIRECT()CURRENT) AND (DC OR DIRECT()CURRENT)
S12         0   VOLTAGE()CONTROL?()RESISTOR?
S13         3   CURRENT()SOURCE?
S14         0   (INTERCONNECTING OR INTER()CONNECTING)()GRID?
S15         0   THREE()SECTION()GRID
File 256:SoftBase:Reviews,Companies&Prods. 82-2004/May
        (c)2004 Info.Sources Inc
```

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Set     Items   Description
S1    6056093   MODEL? ? OR VISUAL? OR DIAGRAM? OR GRAPHIC? OR DISPLAY? OR
            CHART? OR REPRESENT? OR GRAPH? ?
S2         66   POWER()CONVERTER(N)S1
S3    4353936   PLURAL? OR VARIOUS OR SEVERAL OR MULTIPL? OR MANY OR NUMER-
            OUS OR UNLIMITED
S4       4965   (BOARD OR CONTROLLER)(N)S1
S5       3728   PACKAGE? (N)S1
S6       6819   (CHIP? ? OR MICROCHIP OR INTEGRATED()CIRCUIT? OR IC OR RAM
            OR RANDOM()ACCESS()MEMORY OR DRAM? OR SRAM? OR ROM? OR PROM? -
            OR EPROM? OR EEPROM? OR FLASH)(N)S1
S7    3027684   COMPRIS? OR INCLUDE? OR CONTAIN?
S8          0   (BUMP AND GRIND)(N)S1
S9       4357   LOAD(N)S1
S10     10210   CHANNEL(N)S1
S11    260701   (DC OR DIRECT()CURRENT) AND (DC OR DIRECT()CURRENT)
S12       266   VOLTAGE()CONTROL?()RESISTOR?
S13     15744   CURRENT()SOURCE?
S14         9   (INTERCONNECTING OR INTER()CONNECTING)()GRID?
S15         0   THREE()SECTION()GRID
S16        71   (BUMP OR GRIND)(N)S1
S17         0   S2 AND S4 AND S5
S18         0   S2 AND S4
S19         0   S2 AND S5
S20         0   S2 AND S6
S21        12   S5 AND S6
S22         0   S6 AND S7 AND S16
S23         0   S6 AND S16
S24         0   S6 AND S9 AND S10
S25         2   S6 AND S9
S26         8   S6 AND S10
S27         4   S6 AND CHANNEL()MODE?
S28         0   S9 AND S12
S29        18   S9 AND S13
S30      1649   SECTION(N)S1
S31         0   S27 AND S14
S32         0   S27 AND S15
S33       101   S2 OR S14 OR S21OR S25 OR S26 OR S27 OR S29
S34        82   S33 NOT PY>2001
S35        82   S34 NOT PD>20010328
S36        61   RD (unique items)
File   8:Ei Compendex(R) 1970-2004/Jun W1
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File 202:Info. Sci. & Tech. Abs. 1966-2004/May 14
         (c) 2004 EBSCO Publishing
File  65:Inside Conferences 1993-2004/Jun W2
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/Jun W1
         (c) 2004 Institution of Electrical Engineers
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File  94:JICST-EPlus 1985-2004/May W4
         (c)2004 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/May
         (c) 2004 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2004/May W5
         (c) 2004 FIZ TECHNIK
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
```

36/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

08515756 E.I. No: EIP01035587393
Title: High level simulink switch model for investigating capacitive effects
Author: Murphy, C.A.; Krein, P.T.
Corporate Source: Univ of Illinois, Urbana, IL, USA
Conference Title: 7th Workshop on Computers in Power Electronics
Conference Location: Blacksburg, VA, USA Conference Date: 20000716-20000718
Sponsor: IEEE
E.I. Conference No.: 57971
Source: IEEE Workshop on Computers in Power Electronics 2000. IEEE, Piscataway, NJ, USA,00TH8535. p 241-246
Publication Year: 2000
CODEN: IWCEFX ISSN: 1093-5142
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 0105W1
Abstract: Often device capacitance is neglected as a loss path in power converters. In high voltage-low current conditions it can lead to significant power loss as the capacitance is charged and discharged many times a second. Switch models are usually either ideal or include so much detail they slow a converter simulation. This paper presents a behavioral model that fills in between the two extremes. Implemented in Matlab/Simulink the device accounts for resistance and capacitance as well as the antiparallel diode. Switch power loss accounting is also covered. The switch model is then included in a resonant **power converter model** and compared to a prototype converter. A feedback controller for the converter model is also demonstrated. (Author abstract) 12 Refs.
Descriptors: *Power converters; Capacitance; Semiconductor device models; Switching; Computer simulation; Electric resistance; Semiconductor diodes; Feedback control
Identifiers: Simulink switch model; Resonant power converter
Classification Codes:
704.2 (Electric Equipment); 701.1 (Electricity: Basic Concepts & Phenomena); 714.2 (Semiconductor Devices & Integrated Circuits); 723.5 (Computer Applications); 731.1 (Control Systems)
704 (Electric Components & Equipment); 701 (Electricity & Magnetism); 714 (Electronic Components); 723 (Computer Software); 731 (Automatic Control Principles)
70 (ELECTRICAL ENGINEERING); 71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING); 73 (CONTROL ENGINEERING)

36/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05998608 E.I. No: EIP02056845385
Title: Performance indices for a stochastic model of a power electronic converter
Author: Sangswang, Anawach; Nwankpa, Chika O.
Corporate Source: Ctr. for Electric Power Engineering Dept. of Elec. and Comp. Engineering Drexel University, Philadelphia, PA, United States
Conference Title: 27th Annual Conference of the IEEE Industrial Electronics Society IECON'2001
Conference Location: Denver, CO, United States Conference Date: 20011129-20011202
Sponsor: IEEE
E.I. Conference No.: 58960
Source: IECON Proceedings (Industrial Electronics Conference) v 2 2001. p 984-989 (IEEE cat n 01CH37243)
Publication Year: 2001
CODEN: IEPREA

Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 0202W1
Abstract: This paper presents a stochastic model of an inverter with practical uncertainties. The stochastic model is based on the introduction of perturbations in the duty ratio of switching converters as random noise processes, which has been developed by the use of the theory of stochastic differential calculus. The characteristics and performance of a stochastic **power converter model** are evaluated. Attention is mainly focused on finding performance indices, critical energy (E prime //C) and the mean first passage time (MFPT). It is shown that the MFPT provides further insights into inverter's vulnerability due to switching time uncertainties. 9 Refs.
Descriptors: *Electric inverters; Power electronics; Random processes; Mathematical models; Ordinary differential equations; Pulse width modulation; Perturbation techniques; Computer simulation; White noise; Low pass filters
Identifiers: Three-phase inverter; Critical energy; Mean first passage time; Time-invariant system; Stochastic model
Classification Codes:
713.5 (Other Electronic Circuits); 922.1 (Probability Theory); 921.6 (Numerical Methods); 921.2 (Calculus); 723.5 (Computer Applications); 703.2 (Electric Filters)
713 (Electronic Circuits); 922 (Statistical Methods); 921 (Applied Mathematics); 723 (Computer Software, Data Handling & Applications); 703 (Electric Circuits)
71 (ELECTRONICS & COMMUNICATION ENGINEERING); 92 (ENGINEERING MATHEMATICS); 72 (COMPUTERS & DATA PROCESSING); 70 (ELECTRICAL ENGINEERING, GENERAL)

36/5/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05453539 E.I. No: EIP00014966492
Title: Power converter analysis and design using symbolic modelling
Author: Su, Huijuan; Wong, Chi Chung; Payne, Frederick H.
Corporate Source: RMIT Univ, Melbourne, Aust
Conference Title: Proceedings of the 1998 2nd International Conference on Power Electronics Drives and Energy Systems for Industrial Growth, PEDES'98
Conference Location: Perth, Aust Conference Date: 19981201-19981203
Sponsor: CRESTA; Curtin University of Technology; IEEE WA Section; Power Electronics Society; et al.
E.I. Conference No.: 55789
Source: Proceedings of the IEEE International Conference on Power Electronics, Drives and Energy Systems for Industrial Growth, PEDES v 2 1998. p 953-958
Publication Year: 1998
CODEN: 002429
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); X; (Experimental)
Journal Announcement: 0002W3
Abstract: Symbolic modelling is used to **model power converter** circuits such that exact time-domain equations can be derived and used to evaluate / improve the performance of the design. The proposed method works in the time domain and allows steady-state solutions to be sought directly. Both continuous and discontinuous conduction modes can be solved. This method completely eliminates numerical errors usually associated with all numerical methods. Furthermore, the proposed method greatly speeds up analysis and design time. A step-down dc-dc converter system is used as an example to illustrate the application of the method. (Author abstract) 9 Refs.
Descriptors: *Power converters; Computer simulation; Electric network analysis; Electric network synthesis; Time domain analysis; Numerical methods; Switching circuits; Frequency response

Identifiers: Power converter analysis; Symbolic modelling; Steady state solutions; Conduction modes; Dc-dc converters
Classification Codes:
704.2 (Electric Equipment); 723.5 (Computer Applications); 703.1 (Electric Networks); 921.6 (Numerical Methods)
704 (Electric Components & Equipment); 723 (Computer Software); 703 (Electric Circuits); 921 (Applied Mathematics)
70 (ELECTRICAL ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

36/5/4 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05177096 E.I. No: EIP98124489034
Title: Three phase voltage-fed space vector modulated soft-switching PFC rectifier with instantaneous power feedback scheme
Author: Yamamoto, M.; Hattori, S.; Hiraki, E.; Nakaoka, M.; Horiuchi, T.; Sugawara, Y.
Corporate Source: Yamaguchi Univ, Yamaguchi, Jpn
Conference Title: Proceedings of the 1998 7th International Conference on Power Electronics and Variable Speed Drives
Conference Location: London, UK Conference Date: 19980921-19980923
E.I. Conference No.: 49333
Source: IEE Conference Publication n 456 1998. IEE, Stevenage, Engl. p 92-98
Publication Year: 1998
CODEN: IECPB4 ISSN: 0537-9989
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9901W4
Abstract: This paper presents performance evaluations in steady and transient-states of quasi-resonant commutated bridge arm link three phase PFC rectifier with instantaneous power feedback and DC output voltage regulation loops. This three phase PFC rectifier topology is based upon digitally-modulated sinewave space vector processing, which can operate under a principle of ZVS-PWM transition due to auxiliary quasi-resonant commutation circuit incorporated into each three phase bridge arm. In the first place, a practical design of auxiliary resonant commutation circuit with **current source** type **load model** is graphically described on the basis of its state variable analysis. In the second place, the digital control system of three phase voltage-fed soft-switched PWM converter suitable and acceptable for high power utility applications is implemented on the synchronous rotating d-q coordinate axis. Finally, a novel prototype of this three phase PFC rectifier operating at soft-switching PWM strategy is evaluated as compared with hard switching PWM three phase PFC rectifier in terms of computer-aided simulation results. (Author abstract) 7 Refs.
Descriptors: *Power converters; Electric rectifiers; Resonant circuits; Electric power factor correction; Pulse width modulation; Voltage control; Electric commutation; Electric network topology; Electric network synthesis; Digital control systems
Identifiers: Space voltage vector modulation
Classification Codes:
703.1.2 (Electric Network Synthesis)
704.2 (Electric Equipment); 703.1 (Electric Networks); 701.1 (Electricity: Basic Concepts & Phenomena); 731.3 (Specific Variables Control)
704 (Electric Components & Equipment); 703 (Electric Circuits); 701 (Electricity & Magnetism); 731 (Automatic Control Principles)
70 (ELECTRICAL ENGINEERING); 73 (CONTROL ENGINEERING)

36/5/7 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04959517 E.I. No: EIP98034101626
Title: Adaptive passivity-based control of average dc-to-dc power converter models
Author: Sira-Ramirez, Hebertt; Ortega, Romeo; Garcia-Esteban, Mauricio
Corporate Source: Universidad de Los Andes, Merida, Venez
Source: International Journal of Adaptive Control and Signal Processing v 12 n 1 Feb 1998. p 63-80
Publication Year: 1998
CODEN: IACPED ISSN: 0890-6327
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 9804W5
Abstract: An adaptive feedback regulation scheme is proposed for the stabilization of average models of dc-to-dc power converters exhibiting unknown but constant resistive loads. The scheme is based on a dynamical feedback policy which suitably modifies the total energy of the closed-loop system while inducing appropriate damping injections on the desired stabilization error dynamics. The performance of the proposed adaptive regulators is tested through computer simulations including stochastic perturbation inputs. (Author abstract) 29 Refs.
Descriptors: *Adaptive control systems; Closed loop control systems; Feedback control; System stability; Electric loads; Power converters; Stochastic control systems; Computer simulation
Identifiers: Dynamical feedback policy; Stochastic perturbation inputs
Classification Codes:
731.1 (Control Systems); 731.3 (Specific Variables Control); 731.4 (System Stability); 706.1 (Electric Power Systems); 704.2 (Electric Equipment); 723.5 (Computer Applications)
731 (Automatic Control Principles); 706 (Electric Transmission & Distribution); 704 (Electric Components & Equipment); 723 (Computer Software)
73 (CONTROL ENGINEERING); 70 (ELECTRICAL ENGINEERING); 72 (COMPUTERS & DATA PROCESSING)

36/5/9 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03931046 E.I. No: EIP94061300288
Title: Accurate simulation of GaAs MESFET's intermodulation distortion using a new drain-source current model
Author: Pedro, Jose Carlos; Perez, Jorge
Corporate Source: Univ de Aveiro, Aveiro, Port
Source: IEEE Transactions on Microwave Theory and Techniques v 42 n 1 Jan 1994. p 25-33
Publication Year: 1994
CODEN: IETMAB ISSN: 0018-9480
Language: English
Document Type: JA; (Journal Article) Treatment: X; (Experimental); T; (Theoretical); N; (Numerical)
Journal Announcement: 9410W3
Abstract: An accurate characterization of the nonlinear distortion caused by the Ids(Vgs, Vds) current in a MESFET, does not allow the common approach of splitting this nonlinear equivalent circuit element in two voltage dependent nonlinear **current sources** , Gm(Vgs) and Gds(Vds). By an improved laboratory characterization procedure, it was possible to extract the cross terms of the Ids (Vgs, Vds) Taylor Series expansion. Measurements and Volterra Series simulations, made at 2GHz, have shown that they can give an important contribution to the prediction and understanding of MESFET's intermodulation load-pull behavior. (Author abstract) 20 Refs.
Descriptors: *MESFET devices; Nonlinear networks; Amplifiers (electronic); Mathematical models; Intermodulation; Equivalent circuits
Identifiers: Intermodulation distortion; Drain source current **model** ; **Load** pull behavior
Classification Codes:
714.2 (Semiconductor Devices & Integrated Circuits)

is shown to be extremely effective for these simulation studies.

36/5/23 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7106446 INSPEC Abstract Number: B2002-01-1210-007
Title: Study of synchronous DC/DC converters in high-current processor power delivery systems
Author(s): Chickamenahalli, S.A.; Yuan-Liang Li; Figueroa, D.G.
Conference Title: Proceedings 2000 HD International Conference on High-Density Interconnect and Systems Packaging (SPIE Vol.4217) p.182-7
Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Reston, VA, USA
Publication Date: 2000 Country of Publication: USA xvi+617 pp.
ISBN: 0 930815 60 2 Material Identity Number: XX-2001-01667
Conference Title: 2000 HD International Conference on High-Density Interconnect and Systems Packaging
Conference Sponsor: SPIE; IMAPS - Int. Microelectron. & Packaging Soc.; CMP Media
Conference Date: 25-28 April 2000 Conference Location: Denver, CO, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)
Abstract: With the advances in MOSFET technologies, switching a DC/DC converter at several MHz has become rather common. Also, multiple phases of these converters are required in order to meet the increasing transient power requirements of the load. In this paper, the application of a multiple-phase, fully synchronous DC/DC converter model connected to a microprocessor power delivery system is addressed. Performance evaluation of the complete power delivery system based on single and four-phase DC/DC converters is done. Advantages and disadvantages of each design are noted. Comparison is also made for various **load representations** . The **load representations** considered include a piecewise linear **current source** , a time-controlled switch, and a first and second-order polynomial voltage controlled **current source** . Differences in the output characteristics with a simple source replacement of the DC source and with an actual voltage regulator module (VRM) are also highlighted. (8 Refs)
Subfile: B
Descriptors: active networks; DC-DC power convertors; microprocessor chips; piecewise linear techniques; power supply circuits; voltage regulators
Identifiers: synchronous DC/DC converters; high-current processor power delivery systems; MOSFET technologies; DC/DC converter switching; multiple phase converters; load transient power requirements; multiple-phase synchronous DC/DC converter model; microprocessor power delivery system; power delivery system; four-phase DC/DC converters; single-phase DC/DC converters; **load representations** ; piecewise linear **current source** ; time-controlled switch; first-order polynomial voltage controlled **current source** ; second-order polynomial voltage controlled **current source** ; output characteristics; source replacement; DC source; voltage regulator module
Class Codes: B1210 (Power electronics, supply and supervisory circuits); B1265F (Microprocessors and microcomputers); B2570 (Semiconductor integrated circuits); B1160 (Nonlinear network analysis and design); B1270E (Active filters and other active networks)

36/5/24 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7086344 INSPEC Abstract Number: B2001-12-8310D-033, C2001-12-3260B-013
Title: Multilevel modeling and simulation of a switched reluctance machine
Author(s): Pletea, I.-V.; Alexa, D.; Goras, T.
Author Affiliation: Fac. of Electron. & Telecommun., Tech. Univ. of Iasi, Romania

Conference Title: 24th International Spring Seminar on Electronics Technology. Concurrent Engineering in Electronic Packaging. ISSE 2001. Conference Proceedings (Cat. No.01EX492) p.248-52
Editor(s): Dumitrache, I.; Svasta, P.
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA 309 pp.
ISBN: 0 7803 7111 9 Material Identity Number: XX-2001-01303
U.S. Copyright Clearance Center Code: 0 7803 7111 9/91/$10.00
Conference Title: 24th International Spring Seminar on Electronics Technology. Concurrent Engineering in Electronic Packaging. ISSE 2001. Conference Proceedings
Conference Sponsor: Mintr. Educ. & Res.; IEEE Romania Sect.; ARIES - Romanian Assoc. Electron. & Software Ind.; Elma Trenew Electron. SRL; RoundElectr. SRL; Diana SRL; Bere Alutus SA; Boromir SA
Conference Date: 5-9 May 2001 Conference Location: Calimanesti-Caciulata, Romania
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)
Abstract: In this paper, the modeling and simulation of a switched reluctance machine is described. Modeling and simulation is an already accepted method in the design of drive systems. The entire drive, including power converter, SRM, mechanical load and control are modeled in one multilevel model. The paper explains why use is made of a multilevel package for modeling and simulation of a complete drive system. The application of mechatronic systems requires more modeling effort compared to modeling of regular electronic systems. This is caused by the difference in models for the electrical machine, the power converter and the control of the drive. A multilevel model is applied which combines the circuit model, a block diagram and programming language, and thereby eases the modeling process. Due to the required small fine step in the simulation of the power converter, the total simulation time is large. Therefore, a simulation program must used, which has special ideal models for the semiconductor switches and thus reduces total simulation time. Results from the simulation show the internal waveforms of the converter, such as the rotor angle dependent inductance of the stator, angular frequency of the rotor and the torque produced by the SRM. (7 Refs)
Subfile: B C
Descriptors: inductance; machine control; mechatronics; power convertors; power semiconductor switches; power system simulation; reluctance motor drives; torque
Identifiers: multilevel modeling; simulation; switched reluctance machine ; modeling; drive system design; power converter; mechanical load; control; multilevel model; multilevel modeling/simulation package; mechatronic systems; modeling effort; electronic systems; electrical machine model; drive control model; **power converter model** ; circuit model; block diagram; programming language; modeling process; total simulation time; simulation program; ideal models; semiconductor switches; converter internal waveforms; rotor angle dependent inductance; stator; rotor angular frequency; SRM torque
Class Codes: B8310D (Synchronous machines); B8510 (Drives); B2180B (Relays and switches); B2560P (Power semiconductor devices); B8360 (Power convertors and power supplies to apparatus); C3260B (Electric actuators and final control equipment); C3340H (Control of electric power systems); C7410B (Power engineering computing)

36/5/25 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6926877 INSPEC Abstract Number: B2001-06-1265F-076
Title: Study of DC/DC converters in high-performance processor power delivery systems
Author(s): Chickamenahalli, S.A.; Yuan-Liang Li; Figueroa, D.G.
Journal: Advancing Microelectronics vol.28, no.2 p.18-22
Publisher: IMAPS-Int. Microelectron. & Packaging Soc,

Publication Date: March-April 2001 Country of Publication: USA
CODEN: ADMIFA
Material Identity Number: G462-2001-002
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Theoretical (T)
Abstract: With the advances in MOSFET technologies, switching a DC/DC converter at several MHz has become rather common. Also, multiple phases of these converters are required in order to meet the increasing transient power requirements of the load. In this paper, the application of a multiple-phase, fully synchronous DC/DC converter model when connected to a microprocessor power delivery system is addressed. Performance examination of the complete power delivery system based on a single and four-phase DC/DC converter is done. Advantages and disadvantages of each design are noted. Comparison is also made for various **load representations** . The **load representations** considered include a piecewise linear **current source** , a time-controlled switch, and a first and second-order polynomial voltage controlled **current source** . Differences in the output characteristics with a simple source replacement of the DC source and with an actual voltage regulator module (VRM) are also highlighted. (8 Refs)
Subfile: B
Descriptors: active networks; DC-DC power convertors; integrated circuit modelling; lumped parameter networks; microprocessor chips; power supply circuits; voltage regulators
Identifiers: DC/DC converters; processor power delivery systems; MOSFET technologies; DC/DC converter switching; multiple converter phases; load transient power requirements; multiple-phase fully synchronous DC/DC converter model; microprocessor power delivery system; power delivery system; four-phase DC/DC converter; single-phase DC/DC converter; **load representation** ; piecewise linear **current source** ; time-controlled switch; second-order polynomial voltage controlled **current source** ; first-order polynomial voltage controlled **current source** ; output characteristics; source replacement; DC source; voltage regulator module
Class Codes: B1265F (Microprocessors and microcomputers); B1210 (Power electronics, supply and supervisory circuits); B1270E (Active filters and other active networks); B2570A (Semiconductor integrated circuit design, layout, modelling and testing); B1150D (Lumped linear networks)

36/5/26 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6900630 INSPEC Abstract Number: B2001-05-8120L-068
Title: Sensitivity of harmonic load model **parameters to voltage and current waveforms**
Author(s): Gul, O.; Milanovic, J.V.
Author Affiliation: Dept. of Electr. Eng., Istanbul Tech. Univ., Turkey
Conference Title: Ninth International Conference on Harmonics and Quality of Power. Proceedings (Cat. No.00EX441) Part vol.3 p.1041-6 vol.3
Editor(s): Domijan, A.
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA 3 vol. iii+1078 pp.
ISBN: 0 7803 6499 6 Material Identity Number: XX-2001-00027
U.S. Copyright Clearance Center Code: 0 7803 6499 6/2000/$10.00
Conference Title: Proceedings of 2000 International Conference on Harmonics and Quality of Power
Conference Sponsor: Florida Power Affilates Electr. Power Eng. Program; Power Quality Lab at the Univ. Florida; IEEE Power Eng. Soc
Conference Date: 1-4 Oct. 2000 Conference Location: Orlando, FL, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: A generic **load model** for harmonic loads is used in the study. The model consists of resistance, inductance and capacitance connected in parallel with a **current source** . The modelling technique is based on using actual recorded data and it is particularly suitable for

developing aggregate **load models** . The study concentrates on establishing the sensitivity of the load parameters (i.e., R, L and C) to variation in measured voltage and current waveforms. In an attempt to establish the ranges of variation of different parameters various test cases are used including several sets of actual field measurements. (11 Refs)
Subfile: B
Descriptors: capacitance; distribution networks; electric resistance; inductance; load (electric); power system harmonics; sensitivity analysis
Identifiers: harmonic **load model** parameters; current waveforms; voltage waveforms; parameters sensitivity; resistance; inductance; capacitance; **current source** ; modelling; aggregate **load models** ; distribution feeders
Class Codes: B8120L (Power supply quality and harmonics); B8120J (Distribution networks)

36/5/33 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

5883559 INSPEC Abstract Number: B9805-8360-061
Title: Comparisons of loss and switching performance characteristics of IGBTS, MOSFETS and MCTS in resonant power converters
Author(s): Brown, A.J.; Mellor, P.H.; Stone, D.A.
Author Affiliation: Sheffield Univ., UK
Conference Title: Symposium on Power Electronics, Industrial Drives Power Quality, Traction Systems. Proceedings. Speedam p.A1-1-6
Publisher: Univ. `Federico II', Napoli, Italy
Publication Date: 1996 Country of Publication: Italy 2 vol. (x+684+34) pp.
Material Identity Number: XX98-00262
Conference Title: Symposium on Power Electronics, Industrial Drives Power Quality, Traction Systems Proceedings
Conference Date: 5-7 June 1996 Conference Location: Capri, Italy
Availability: Prof A Del Pizzo, SPEEDAM, c/o Dip di Ingegneria Elettrica, Universita `Federico II', via Claudio 21, I-80125 Napoli, Italy
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: The paper compares the efficiency and switching characteristics of power IGBTs, MOSFETs and MCTs for use in resonant soft-switching power converters for low voltage and medium current traction applications. The losses in **representative power converter** poles are measured calorimetrically, from which comparisons are drawn between the different device technologies and the benefits of hard and soft switching. (8 Refs)
Subfile: B
Descriptors: MOS-controlled thyristors; power bipolar transistors; power MOSFET; power semiconductor switches; resonant power convertors; switching circuits; thyristor convertors; traction
Identifiers: resonant soft-switching power converters; traction applications; efficiency; switching characteristics; power IGBTs; power MOSFETs; power MCTs
Class Codes: B8360 (Power convertors and power supplies to apparatus); B1210 (Power electronics, supply and supervisory circuits); B2560J (Bipolar transistors); B2560R (Insulated gate field effect transistors); B2560L (Thyristors and silicon controlled rectifiers); B8520 (Transportation)

36/5/34 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

5862361 INSPEC Abstract Number: B9804-8360-095, C9804-7410B-063
Title: A controlled current source **model for a multipulse converter**

drive using EMTP
Author(s): Varadan, S.; Makram, E.B.
Author Affiliation: Dept. of Electr. & Comput. Eng., Clemson Univ., SC, USA
Conference Title: Proceedings of the ICHQP. 7th International Conference on Harmonics and Quality of Power p.764-9
Publisher: Univ. Nevada Las Vegas, Las Vegas, NV, USA
Publication Date: 1996 Country of Publication: USA x+790 pp.
Material Identity Number: XX96-02265
Conference Title: Proceedings of International Conference on Harmonics and Quality of Power
Conference Sponsor: IEEE Power Eng. Soc.; Nevada Power Co.; Univ. Nevada Las Vegas
Conference Date: 16-18 Oct. 1996 Conference Location: Las Vegas, NV, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: This paper presents a new time-domain **current source** model for a multi-pulse power converter drive. The controlled **current source** (CCS) depends on the DC side load (machine resistance, inductance and back EMF/speed), the AC side bus voltage and the operating condition of the power converter drive (firing angle). The proposed **load model** is simulated using the Transient Analysis of Control Systems (TACS) feature of the Electro Magnetic Transients Program (EMTP) and the switching action of the thyristors is accommodated by means of thyristor functions. The model is validated by means of a comparison with simulations obtained from the Electro Magnetic Transients Program (EMTP) where the converter drive is treated as a load with each thyristor represented as a time controlled switch. The major advantage of the proposed model is that for every T thyristors present only T/2 thyristor functions are needed. In order that a comparison of the proposed model with the guidelines in the IEEE Standards 519 be performed, the total current harmonic distortion is studied as a function of several parameters that include: converter firing angle (a); DC side load current; DC side back EMF/machine dynamics; and bus voltage anomalies such as harmonics and unbalance. (8 Refs)
Subfile: B C
Descriptors: circuit analysis computing; DC motor drives; electric machine analysis computing; harmonic distortion; machine theory; power convertors; power supplies to apparatus; power system analysis computing; power system harmonics; software packages
Identifiers: multi-pulse power converter; time-domain **current source** model; controlled **current source** ; DC side load; TACS; EMTP; thyristors; IEEE Standards 519; total current harmonic distortion; computer simulation; DC motor drive; power supply
Class Codes: B8360 (Power convertors and power supplies to apparatus); B8510 (Drives); B8320 (d.c. machines); B1130B (Computer-aided circuit analysis and design); C7410B (Power engineering computing); C7410D (Electronic engineering computing)

36/5/39 (Item 17 from file: 2)
DIALOG(R)File 2:INSPEC

5697673 INSPEC Abstract Number: B9710-8360-254, C9710-7410B-156
Title: A transient behavioral model (TBM) for power converters
Author(s): Kaglawala, R.; Venkata, S.S.; Lauritzen, P.O.; Sundaram, A.; Adapa, R.
Author Affiliation: Washington Univ., Seattle, WA, USA
Conference Title: 1996 IEEE Workshop on Computers in Power Electronics. 5th IEEE Workshop on Computers in Power Electronics (Cat. No.96TH8288) p.18-24
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA iv+181 pp.
ISBN: 0 7803 3977 0 Material Identity Number: XX97-01980
U.S. Copyright Clearance Center Code: 0 7803 3977 0/96/$10.00

Conference Title: 5th IEEE Workshop on Computers in Power Electronics
Conference Sponsor: IEEE Power Electron. Soc
Conference Date: 11-14 Aug. 1996 Conference Location: Portland, OR, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: This paper describes a new technique to model power converters. The resulting **power converter model** is referred to as a transient behavioral model (TBM). First, a simple buck power converter is used to demonstrate the TBM. A power converter called the dynamic voltage restorer is used to demonstrate a practical application of the TBM. It is shown that the TBM yields simulation results almost as accurate as the ideal switch model (ISM). At the same time, the TBM is computationally more efficient than the ISM. These features, coupled with the simplicity and the ease of implementation in a standard circuit simulator, make the TBM an attractive alternative to the ISM. (16 Refs)
Subfile: B C
Descriptors: circuit analysis computing; power convertors; power engineering computing
Identifiers: buck power converter; dynamic voltage restorer; transient behavioral model; circuit modelling; application; ideal switch model; computational efficiency; circuit simulator; CPU time; computer simulation
Class Codes: B8360 (Power convertors and power supplies to apparatus); B1210 (Power electronics, supply and supervisory circuits); B1130B (Computer-aided circuit analysis and design); C7410B (Power engineering computing); C7410D (Electronic engineering computing)

36/5/42 (Item 20 from file: 2)
DIALOG(R)File 2:INSPEC

5490367 INSPEC Abstract Number: B9703-8520-036
Title: Automated state-space simulation of small-scale and vehicular electric power systems
Author(s): Mayer, J.S.; Griffith, D.A.
Author Affiliation: Dept. of Electr. Eng., Pennsylvania State Univ., University Park, PA, USA
Conference Title: IECEC 96. Proceedings of the 31st Intersociety Energy Conversion Engineering Conference (Cat. No.96CH35978) Part vol.3 p. 1913-18 vol.3
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA 4 vol. (xvi+xvii+xiv+vi+2372) pp.
ISBN: 0 7803 3547 3 Material Identity Number: XX96-03032
U.S. Copyright Clearance Center Code: 0 7803 3547 3/96/7/16$4.00
Conference Title: IECEC 96. Proceedings of the 31st Intersociety Energy Conversion Engineering Conference
Conference Sponsor: IEEE Natl. Capital Area Council
Conference Date: 11-16 Aug. 1996 Conference Location: Washington, DC, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: The design of increasingly complex electromechanical systems containing AC machine-power converter subsystems requires efficient methods of simulating the machine and power converter dynamics. While circuit-oriented simulations can be used for this application, state-space methods offer greater flexibility in modeling the nonelectrical components and in the choice of integration algorithms and software. State-space methods have the disadvantage, however, of requiring special attention when interconnecting individual component models to represent an overall system. In this paper, a state-space **power converter model** that can be readily connected with other component model and which is computationally efficient is obtained using a combination of circuit (graph) theory and reference frame transformations. An alternator-rectifier that is part of a pulse-power system is used to demonstrate the model and its implementation.

In addition, an automated tool which handles the task of assembling a system simulation from a library of component models is described. (9 Refs)
Subfile: B
Descriptors: AC machines; AC-DC power convertors; circuit analysis computing; electric machine analysis computing; electric vehicles; graph theory; rectifying circuits; state-space methods
Identifiers: vehicular electric power systems; state-space simulation; AC machine-power converter subsystems; integration algorithms; software; graph theory; pulse-power system; computer simulation; alternator-rectifier system
Class Codes: B8520 (Transportation); B8310 (a.c. machines); B8360 (Power convertors and power supplies to apparatus); B1210 (Power electronics, supply and supervisory circuits); B0250 (Combinatorial mathematics); B8320 (d.c. machines); B1130B (Computer-aided circuit analysis and design)

36/5/43 (Item 21 from file: 2)
DIALOG(R)File 2:INSPEC

5406121 INSPEC Abstract Number: B9612-8360-079, C9612-3340H-066
Title: mu -synthesis of a robust voltage controller for a Buck-Boost converter
Author(s): Buso, S.
Author Affiliation: Dipartimento di Elettronica e Inf., Padova Univ., Italy
Conference Title: PESC 96 Record. 27th Annual IEEE Power Electronics Specialists Conference (Cat. No.96CH35962) Part vol.1 p.766-72 vol.1
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA 2 vol. xxiv+2000 pp.
ISBN: 0 7803 3500 7 Material Identity Number: XX96-02749
U.S. Copyright Clearance Center Code: 0 7803 3500 7/96/$5.00
Conference Title: PESC Record. 27th Annual IEEE Power Electronics Specialists Conference
Conference Sponsor: IEEE Power Electron. Soc.; Univ. degli Studi di Milano
Conference Date: 23-27 June 1996 Conference Location: Baveno, Italy
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: This paper proposes the structured singular value (mu) approach to the problem of designing an output voltage regulator for a buck-boost power converter with current mode control. This approach allows a quantitative description of the effects of reactive component tolerances and operating point variations, which strongly affect the power converter dynamics. At first, a suitable linear **power converter model** is derived, whose parameter variations are described in terms of perturbations of the linear fractional transformation (LFT) class. Then, mu -analysis is used to evaluate the robustness of a conventional PI voltage regulator with respect to the modeled perturbations. Finally, the approximated mu -synthesis procedure, known as D-K iteration, is used to design a regulator ensuring robust performance. Simulated results are presented, describing the small and large signal behaviour of a reduced-order approximation of the mu -synthesised controller. (7 Refs)
Subfile: B C
Descriptors: control system analysis; control system synthesis; DC-DC power convertors; iterative methods; robust control; voltage control; voltage regulators
Identifiers: robust voltage controller; mu -synthesis; structured singular value approach; control design; output voltage regulator; current mode control; reactive component tolerances; operating point variations; control simulation; power converter dynamics; linear **power converter model** ; perturbations; linear fractional transformation class; D-K iteration; robust performance; small signal behaviour; large signal

behaviour; reduced-order approximation; buck-boost power converter
Class Codes: B8360 (Power convertors and power supplies to apparatus); B1210 (Power electronics, supply and supervisory circuits); C3340H (Control of electric power systems); C3110B (Voltage control); C3220 (Controllers); C1320 (Stability in control theory); C1310 (Control system analysis and synthesis methods)

36/5/44 (Item 22 from file: 2)
DIALOG(R)File 2:INSPEC

5347794 INSPEC Abstract Number: B9609-8360-067, C9609-3340H-185
Title: High voltage rectifiers-multilevel inverters cascade. Application to asynchronous machine field oriented control
Author(s): Berkouk, M.; Romdhane, Y.B.; Manesse, G.
Author Affiliation: Lab. d'Electr. Ind., CNAM, Paris, France
Conference Title: Stockholm Power Tech International Symposium on Electric Power Engineering Part vol.3 p.125-33 vol.3
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA 6 vol. (iii+261+iv+272+vii+448+viii+551+xii+843+vi+385) pp.
Material Identity Number: XX96-01932
Conference Title: Proceedings of Stockholm Power Tech International Symposium on Electric Power Engineering
Conference Date: 18-22 June 1995 Conference Location: Stockholm, Sweden
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: The object of this paper is to present a synchronous PWM rectifier/three-level voltage inverter/three-phase induction motor drive set. The authors present models of each power converter of this set using Petri nets. Then, they expose three control strategies for the three-level voltage inverters. One solution to the problem of the middle point of the inverter input DC-voltage source is also presented. This solution uses one or two synchronous PWM rectifiers. To ameliorate this solution, a control loop of the output voltage of this synchronous PWM rectifier is proposed. This synchronous PWM rectifier/three-level voltage inverter/three-phase induction motor set is used with the field-oriented control of an induction machine. The results of this drive system are given. (17 Refs)
Subfile: B C
Descriptors: AC-DC power convertors; control system analysis; DC-AC power convertors; feedback; induction motor drives; invertors; machine control; machine theory; Petri nets; PWM power convertors; rectifying circuits; voltage control
Identifiers: synchronous PWM rectifier; three-level voltage inverter; three-phase induction motor drive; **power converter models** ; Petri nets ; voltage control strategies; input DC-voltage source middle point; output voltage control loop; field-oriented control; control simulation
Class Codes: B8360 (Power convertors and power supplies to apparatus); B1210 (Power electronics, supply and supervisory circuits); B8510 (Drives); B8310E (Asynchronous machines); B0250 (Combinatorial mathematics); C3340H (Control of electric power systems); C3110B (Voltage control); C1160 (Combinatorial mathematics); C1310 (Control system analysis and synthesis methods)

36/5/45 (Item 23 from file: 2)
DIALOG(R)File 2:INSPEC

5138404 INSPEC Abstract Number: B9601-8110B-104, C9601-3340H-131
Title: Plant models for VAr control with emphasis on DC converters
Author(s): Ostrup, T.; Thanawala, H.; Povh, D.; Liss, G.; Holmberg, D.; Falck Christensen, J.

Conference Title: Proceedings of the 35th Session. International Conference on Large High Voltage Electric Systems Part vol.2 p. 38-306/1-6 vol.2
Publisher: CIGRE, Paris, France
Publication Date: 1995 Country of Publication: France 2 vol. 1426+1240 pp.
Conference Title: Proceedings of CIGRE 35th International Conference on Large High Voltage Electric Systems
Conference Date: 28 Aug.-3 Sept. 1994 Conference Location: Paris, France
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: This report, emphasizing DC power converters, describes the models needed to improve VAr control in power systems. It is based on the technical brochure "Use of DC converters for VAr control" made by Cigre Task Force 38.01.05. The steady-state capability diagram of a typical DC power converter is discussed in the report, and it is shown that in practice the possible area of operation in this is quite small. Different methods to obtain a larger range for reactive power control are mentioned and it is shown how the steady-state models can be used for planning purposes. Finally, different needs regarding the details in the dynamic **power converter models** and the different types of models corresponding to this are mentioned. (2 Refs)
Subfile: B C
Descriptors: control system analysis; power convertors; power system control; reactive power control; voltage control
Identifiers: power systems; VAr control; DC power converters; Cigre; steady-state capability diagram; voltage control analysis; reactive power control; steady-state models; planning; dynamic **power converter models**
Class Codes: B8110B (Power system management, operation and economics); B8360 (Power convertors and power supplies to apparatus); C3340H (Control of electric power systems); C3110B (Voltage control); C3110E (Power and energy control); C1310 (Control system analysis and synthesis methods)

36/5/46 (Item 24 from file: 2)
DIALOG(R)File 2:INSPEC

4986967 INSPEC Abstract Number: B9508-8360-019, C9508-3340H-063
Title: Simulations of the pulse-density modulated resonant converter
Author(s): Zadravec, D.; Mihalic, F.; Milanovic, M.; Jezernik, K.
Author Affiliation: Fac. of Tech. Sci., Maribor Univ., Slovenia
Conference Title: EDPE '94. Proceedings of the 8th International Conference on Electrical Drives and Power Electronics p.92-5
Editor(s): Bencic, Z.; Peric, N.; Rajkovic, B.; Srb, N.
Publisher: KoREMA, Zagreb, Croatia
Publication Date: 1994 Country of Publication: Croatia xiv+290 pp.
Conference Title: EDPE '94. Proceedings of the 8th International Conference on Electrical Drives and Power Electronics
Conference Sponsor: Minist. Sci. & Technol.; Minst. Econ.; KONCAR - Elect. Ind.; et al
Conference Date: 12-14 Sept. 1994 Conference Location: Pula, Croatia
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: The simulation of the controlled HF AC-link resonant power converter with bidirectional switches is shown in the paper. The main-side power converter controller fulfills the requirements of sinusoidal input currents, zero voltage switching and nearly constant resonant voltage amplitude. At the load side, a three-phase on-off current controller is implemented. The zero voltage switching technique (ZVS) reduces the switching losses and introduces a modulation strategy called pulse density modulation (PDM). Simulations of the complete **power converter model** and of the simplified model are made. Based on the simulation results, system dynamic behaviour is analysed. (5 Refs)
Subfile: B C

Descriptors: control system analysis; control system synthesis; electric current control; load (electric); network analysis; power semiconductor switches; pulse modulation; resonant power convertors; switching circuits
Identifiers: HF AC-link resonant power converter; pulse density modulation; PDM; zero voltage switching; ZVS; bidirectional switches; sinusoidal input current; resonant voltage amplitude; load side; three-phase on-off current controller; simulation; dynamic behaviour; control design
Class Codes: B8360 (Power convertors and power supplies to apparatus); B1210 (Power electronics, supply and supervisory circuits); B2560 (Semiconductor devices); B1130 (General circuit analysis and synthesis methods); C3340H (Control of electric power systems); C3110D (Current control); C1310 (Control system analysis and synthesis methods)

36/5/47 (Item 25 from file: 2)
DIALOG(R)File 2:INSPEC

4956209 INSPEC Abstract Number: B9507-8120G-002, C9507-7410B-039
Title: EMTP simulation of an HVDC rectifier operating with a weak AC system
Author(s): Khatri, V.; Sood, V.; Jin, H.
Author Affiliation: Dept. of Electr. & Comput. Eng., Concordia Univ., Montreal, Que., Canada
p.91-5
Publisher: IEEE, New York, NY, USA
Publication Date: 1994 Country of Publication: USA v+354 pp.
ISBN: 0 7803 2091 3
U.S. Copyright Clearance Center Code: 0 7803 2091 3/94/$1.00
Conference Title: Proceedings of 1994 IEEE Workshop on Computers in Power Electronics
Conference Sponsor: IEEE Power Electron. Soc
Conference Date: 7-10 Aug. 1994 Conference Location: Trois-Rivieres, Que., Canada
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: The study of the transient performance of an HVDC power converter using EMTP requires detailed modelling of the controls and power system elements. Furthermore, owing to the complexities associated with EMTP, considerable care has to be exercised during simulation. These requirements take on added importance particularly when the HVDC power converter is operated with a weak AC power system. This paper looks at the impact of the gate firing unit, the valve snubber in the **power converter model** and the initialization technique when operating a rectifier with a weak AC power system. (11 Refs)
Subfile: B C
Descriptors: AC-DC power convertors; circuit analysis computing; digital simulation; HVDC power convertors; power system analysis computing; rectifying circuits; snubbers; software packages; thyristor convertors
Identifiers: HVDC rectifier; HVDC power converter; EMTP; weak AC power system; computer simulation; gate firing unit; valve snubber; initialization technique; DC/AC; thyristors
Class Codes: B8120G (d.c. transmission); B8360 (Power convertors and power supplies to apparatus); B1210 (Power electronics, supply and supervisory circuits); B1130B (Computer-aided circuit analysis and design); C7410B (Power engineering computing); C7410D (Electronic engineering computing)

36/5/48 (Item 26 from file: 2)
DIALOG(R)File 2:INSPEC

4955950 INSPEC Abstract Number: B9507-8360-006

Title: A step-down converter with limited duty cycle range
Author(s): Himmelstoss, F.A.; Frank, H.; Zach, F.C.
Author Affiliation: Power Electron. Sect., Tech. Univ. Wien, Austria
Part vol.1 p.232-7 vol.1
Publisher: IEEE, New York, NY, USA
Publication Date: 1994 Country of Publication: USA 3 vol. xxxvii+2154 pp.
ISBN: 0 7803 1328 3
U.S. Copyright Clearance Center Code: 0 7803 1328 3/94/$03.00
Conference Title: Proceedings of IECON'94 - 20th Annual Conference of IEEE Industrial Electronics
Conference Sponsor: Ind. Electron. Soc. IEEE; Soc. Instrum. & Control Eng. Japan; Electr. & Electron. Assoc. Italy
Conference Date: 5-9 Sept. 1994 Conference Location: Bologna, Italy
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T); Experimental (X)
Abstract: A special step-down power converter is investigated. The basic function, the stationary relationships, the small-signal behavior, the position of the poles and zeros and the dimensioning are treated. Furthermore, for a **model power converter** , simulation and measurement results are compared. Step responses are given as well as dimensioning guidelines. (13 Refs)
Subfile: B
Descriptors: circuit testing; DC-DC power convertors; network analysis; poles and zeros; step response
Identifiers: step-down power converter; limited duty cycle range; small-signal behavior; basic function; stationary relationships; poles and zeros position; dimensioning; simulation; measurement; step responses; guidelines; DC/DC
Class Codes: B8360 (Power convertors and power supplies to apparatus); B1210 (Power electronics, supply and supervisory circuits); B1130 (General circuit analysis and synthesis methods)

36/5/49 (Item 27 from file: 2)
DIALOG(R)File 2:INSPEC

4939710 INSPEC Abstract Number: B9506-8360-045
Title: On the low-frequency noise of DC-to-DC converters with random-switching control
Author(s): Tanaka, T.; Ninomiya, T.; Yoshida, H.
Author Affiliation: Dept. of Electr. & Electron. Eng., Kagoshima Univ., Japan
p.451-6
Publisher: IEEE, New York, NY, USA
Publication Date: 1994 Country of Publication: USA xviii+690 pp.
ISBN: 0 7803 2034 4
U.S. Copyright Clearance Center Code: 0 7803 2034 4/94/$4.00
Conference Title: Proceedings of Intelec 94
Conference Sponsor: Power Electron. Soc. IEEE
Conference Date: 30 Oct.-3 Nov. 1994 Conference Location: Vancouver, BC, Canada
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T); Experimental (X)
Abstract: The low-frequency output noise that is caused by introducing random-switching control into the DC-to-DC power converter is discussed quantitatively. A modified **power converter model** involving the unintended effect of random switching is derived from the consideration of noise-generation mechanisms. After a theoretical analysis based on the model, it is clarified that the magnitude of output noise is in proportion to the variance of switching interval. Experimental results from a buck-type power converter are compared with those obtained theoretically, so that the validity of the theoretical results is confirmed. (4 Refs)
Subfile: B
Descriptors: circuit noise; circuit testing; DC-DC power convertors;

network analysis; power system harmonics; switching circuits
Identifiers: DC-to-DC power converter; buck-type power converter; random-switching control; LF noise; noise-generation mechanisms; model; magnitude; switching interval variance; harmonics
Class Codes: B8360 (Power convertors and power supplies to apparatus); B1210 (Power electronics, supply and supervisory circuits); B1130 (General circuit analysis and synthesis methods)

36/5/50 (Item 28 from file: 2)
DIALOG(R)File 2:INSPEC

4873998 INSPEC Abstract Number: B9503-8360-087
Title: Fourth order DC-DC converters with limited duty cycle range
Author(s): Himmelstoss, F.A.
Author Affiliation: Power Electron. Section, Tech. Univ. of Vienna, Austria
Part vol.1 p.358-64 vol.1
Publisher: IEEE, New York, NY, USA
Publication Date: 1993 Country of Publication: USA 2 vol. (xxxxii+487+470) pp.
ISBN: 0 7803 1842 0
Conference Title: Proceedings of Intelec 93: 15th International Telecommunications Energy Conference
Conference Sponsor: IEEE PELS; IEEE French Sect
Conference Date: 27-30 Sept. 1993 Conference Location: Paris, France
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: Twelve fourth-order PWM DC/DC power converters with limited duty cycle range are treated and a survey of important data (maximum voltage and current ratings for the elements, RMS values for the semiconductor devices and a rough approximation of the losses) of the circuits are given to help to decide whether a given topology is interesting for realization. Furthermore, idealized **power converter models** based on duty ratio averaging are established in which continuous operation mode and ideal devices are assumed. Finally, dimensioning equations for the inductors and the capacitors are given. The results make it possible to estimate the applicability of given power converter structures and offer sufficient material for the calculation and analysis of these circuits. (12 Refs)
Subfile: B
Descriptors: approximation theory; DC-DC power convertors; losses; network analysis; network topology; power capacitors; power inductors; power semiconductor devices; PWM power convertors
Identifiers: fourth-order PWM DC/DC power converters; limited duty cycle range; maximum voltage rating; maximum current rating; RMS values; semiconductor devices; losses approximation; topology; duty ratio averaging ; continuous operation mode; inductors; capacitors
Class Codes: B8360 (Power convertors and power supplies to apparatus); B1210 (Power electronics, supply and supervisory circuits); B8350 (Transformers and reactors); B8390 (Other power apparatus and electric machines); B2140 (Inductors and transformers); B1110 (Network topology); B1130 (General circuit analysis and synthesis methods); B0290F (Interpolation and function approximation); B2560 (Semiconductor devices)

36/5/51 (Item 29 from file: 2)
DIALOG(R)File 2:INSPEC

4834613 INSPEC Abstract Number: B9501-8510-023, C9501-3340H-067
Title: Sliding mode control in comparison with other current control methods for a permanent excited synchronous machine
Author(s): Brosse, A.; Brunsbach, B.J.; Henneberger, G.

Author Affiliation: Tech. Hochschule Aachen, Germany
p.526-31
Publisher: IEE, London, UK
Publication Date: 1994 Country of Publication: UK xix+715 pp.
Conference Title: Proceedings of 5th International Conference on Power Electronics and Variable-Speed Drives
Conference Date: 26-28 Oct. 1994 Conference Location: London, UK
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)
Abstract: Modern electrical drives require high stationary precision and high dynamics. The power converter is one component of the drive which limits the stationary precision of the drive. The finite switching rate causes current and load ripple which has a direct effect on the accuracy of the speed. The control strategy for the power converter has an essential influence on the ripple of the current as well. Sliding mode control is a control method which takes into consideration that the switching elements of the **power converter represent** discontinuities. Therefore sliding mode control might offer better qualities of the drive than other power converter control strategies. Although sliding mode has already been dealt with in several publications, so far no comparison between sliding mode control and other power converter control strategies has been published. This paper presents such a comparison and both simulation and practical results are given. (5 Refs)
Subfile: B C
Descriptors: electric current control; exciters; machine control; permanent magnet motors; power convertors; switching circuits; synchronous motor drives; variable structure systems
Identifiers: permanent excited synchronous machine; current control; sliding mode control; power converter; finite switching rate; load ripple; current ripple; switching elements; simulation
Class Codes: B8510 (Drives); B8310D (Synchronous machines); B8360 (Power convertors and power supplies to apparatus); C3340H (Control of electric power systems); C1340B (Multivariable control systems); C3110D (Current control)

36/5/52 (Item 30 from file: 2)
DIALOG(R)File 2:INSPEC

4610480 INSPEC Abstract Number: B9404-8110-016
Title: Probabilistic modelling of current harmonics produced by an AC/DC converter under voltage unbalance
Author(s): Yaw-Juen Wang; Pierrat, L.
Author Affiliation: Grenoble Electrotech. Lab., Domaine Univ., St. Martin d'Heres, France
Journal: IEEE Transactions on Power Delivery vol.8, no.4 p.2060-6
Publication Date: Oct. 1993 Country of Publication: USA
CODEN: ITPDE5 ISSN: 0885-8977
U.S. Copyright Clearance Center Code: 0885-8977/93/$03.00
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: Harmonic currents generated by an AC/DC power converter are subject to random variations due partly to fluctuation of the converter's DC load and partly to power source disturbances. The latter are also responsible for the generation of uncharacteristic harmonics. Based on an analytical **power converter model** and probabilistic models of voltage unbalance and converter load variations, the random behaviour of both characteristic and uncharacteristic power system harmonics produced by a six-pulse AC/DC power converter undervoltage unbalance is analyzed. The probability density functions of the magnitude and the phase angle of harmonic currents are derived and compared with the results obtained from Monte Carlo simulations. It is found that the developed probabilistic harmonic model agrees very well with the results of Monte Carlo simulations and gives significant insight into the effects of voltage unbalance and converter DC load variations upon the random properties of the power converter current spectrum. (22 Refs)

Subfile: B
Descriptors: load (electric); Monte Carlo methods; power convertors; power system harmonics; probability
Identifiers: AC/DC power converter; power system harmonics; probabilistic modelling; current harmonics; undervoltage unbalance; DC load; power source disturbances; load variations; six-pulse; probability density functions; phase angle; Monte Carlo simulations; current spectrum
Class Codes: B8110 (Power systems); B8360 (Power convertors and power supplies to apparatus); B0240G (Monte Carlo methods)

36/5/53 (Item 31 from file: 2)
DIALOG(R)File 2:INSPEC

4577338 INSPEC Abstract Number: B9402-8360-157
Title: Elementary working point analysis for DC/DC converters shown for a fourth order buck converter
Author(s): Himmelstoss, F.A.; Zach, F.C.
Author Affiliation: Tech. Univ. of Vienna, Austria
Conference Title: ISIE'93 - Budapest. IEEE International Symposium on Industrial Electronics. Conference Proceedings (Cat.No.93TH0540-5) p. 786-90
Publisher: IEEE, New York, NY, USA
Publication Date: 1993 Country of Publication: USA 794 pp.
ISBN: 0 7803 1227 9
U.S. Copyright Clearance Center Code: 0 7803 1227 9/93/$3.00
Conference Sponsor: IEEE; EPRI; Hungarian Electrotech. Assoc.; Hungarian Acad. Sci.; et al
Conference Date: 1-3 June 1993 Conference Location: Budapest, Hungary
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: A fourth order step-down power converter is treated as an example of how to survey a given circuit to decide whether a given topology is interesting for realization. An idealized **power converter model** is then established in which continuous operation mode and ideal devices are assumed. (9 Refs)
Subfile: B
Descriptors: network analysis; power convertors
Identifiers: network analysis; DC/DC; buck; fourth order step-down power converter; topology; model; continuous operation mode
Class Codes: B8360 (Power convertors and power supplies to apparatus); B1210 (Power electronics, supply and supervisory circuits); B1130 (General analysis and synthesis methods)

36/5/54 (Item 32 from file: 2)
DIALOG(R)File 2:INSPEC

03628173 INSPEC Abstract Number: B90040462
Title: Whoever writes, stays
Author(s): Huber, W.
Journal: Elektronik Praxis vol.25, no.4 p.42-6
Publication Date: 15 Feb. 1990 Country of Publication: West Germany
CODEN: EKPXAM ISSN: 0341-5783
Language: German Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The author reports on the abilities of the latest digital techniques in recording measurements using 'smart' multi-channel plotters. In particular he describes the vertical and flat-bed plotters in YEW's LR range of products. He describes the recording techniques involved, the manner in which the measurements are processed and the storage of data. He mentions paper feed, measurement range, cost per **channel , displays , IC** memory cards, programming, and microprocessor control and comments on important functions (e.g. scaling). (0 Refs)
Subfile: B

Descriptors: digital instrumentation; plotters
Identifiers: YEW LR range; digital techniques; multi-channel plotters; flat-bed plotters; recording techniques; paper feed; measurement range; displays; IC memory cards; programming; microprocessor control
Class Codes: B7250G (Display, recording and indicating instruments)

36/5/55 (Item 33 from file: 2)
DIALOG(R)File 2:INSPEC

03557659 INSPEC Abstract Number: B90013039, C90016573
Title: Digital real-time simulation of a power-converter system
Author(s): Rathjen, O.
Author Affiliation: Tech. Univ. of Braunschweig, West Germany
Conference Title: ESC 89. Proceedings of the 3rd European Simulation Congress p.412-18
Editor(s): Murray-Smith, D.; Stephenson, J.; Zobel, R.N.
Publisher: SCS Eur, Ghent, Belgium
Publication Date: 1989 Country of Publication: Belgium xiii+846 pp.
ISBN: 0 911801 60 x
Conference Sponsor: SCS
Conference Date: 5-8 Sept. 1989 Conference Location: Edinburgh, UK
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)
Abstract: Digital real-time simulation of power converters requires adequate integration algorithms and a powerful computer structure to meet the stringent computational demands. A parallel processing system was developed, consisting of identical vector processing units with local memory. Considering the numerical integration of ordinary differential equations resulting in fine grained parallelism, a bus structure offering high bandwidth and an effective mechanism for interprocessor communication are provided. The real-time simulator was designed to interact with external hardware, e.g. controllers, thus enabling control studies with a typical and **representative power converter** application, a two-terminal HVDC (high voltage direct current) link. (14 Refs)
Subfile: B C
Descriptors: digital simulation; power convertors; power engineering computing; real-time systems
Identifiers: digital real-time simulation; two-terminal HVDC link; power-converter system; integration algorithms; parallel processing system; vector processing units; local memory; numerical integration; ordinary differential equations; fine grained parallelism; bus structure; bandwidth; interprocessor communication; real-time simulator; external hardware; high voltage direct current
Class Codes: B8360 (Power convertors and power supplies to apparatus); C7410B (Power engineering)

36/5/56 (Item 34 from file: 2)
DIALOG(R)File 2:INSPEC

03539697 INSPEC Abstract Number: B90013341, C90005886
Title: Thyristor converters for machine tool main drives with advanced information-processing electronics
Author(s): Leuschner, T.; Menzel, D.
Author Affiliation: VEB Elektroprojekt und Anlagenbau Berlin, Werk Ind. Elektronik Berlin, East Germany
Journal: Technical Information. Process Automation - Electrical Power Installations no.18 p.63-4
Publication Date: April 1989 Country of Publication: East Germany
CODEN: TIPIEU
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P)
Abstract: The scope of application of variable-speed drives with DC motors has expanded technologically and economically thanks to the

extraordinary progress in the development of power and information electronics. Users can now choose from a great variety of **power converter models** . The authors show how the advanced thyristor power converters for D.C. motors, offered by VEB Elektroprojekt und Anlagenbau Berlin (EAB), make possible optimum solutions for all drive problems. (0 Refs)
Subfile: B C
Descriptors: DC motors; machine control; machine tools; power convertors; thyristor applications; variable speed drives; velocity control
Identifiers: machine control; machine tool; variable-speed drives; electronics; thyristor power converters; D.C. motors
Class Codes: B8620 (Manufacturing industries); B8510 (Drives); B8320 (d.c. machines); B8360 (Power convertors and power supplies to apparatus); C3340H (Electric systems); C3355C (Machining processes and machine tools); C3120E (Velocity, acceleration and rotation)

36/5/57 (Item 35 from file: 2)
DIALOG(R)File 2:INSPEC

02725835 INSPEC Abstract Number: B86056760
Title: No- load model **of an induction motor fed from a constant-voltage or** current source **for various types of primary winding connections**
Author(s): Bill, K.; Pawluk, K.
Author Affiliation: Dept. of Fundamental Res. in Electrotech., Electrotech. Inst., Warszawa, Poland
Journal: Prace Instytutu Elektrotechniki vol.33, no.137 p.93-106
Publication Date: 1985 Country of Publication: Poland
CODEN: PIELA4 ISSN: 0032-6216
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: A model is based on a combination of field and circuit theory adapted to the investigation of induction motor field and circuit quantities. Terminal voltage or currents, type of primary winding connections, nonlinearity of the B-H curve and mutual rotor and stator positions are taken into account. (8 Refs)
Subfile: B
Descriptors: circuit theory; constant **current sources** ; electromagnetic field theory; induction motors; machine theory; machine windings
Identifiers: no- **load model** ; constant-voltage source; constant- **current source** ; circuit theory; induction motor; primary winding connections; B-H curve; mutual rotor and stator positions
Class Codes: B1190 (Other and miscellaneous); B5140 (Electromagnetic induction); B8310E (Asynchronous machines)

36/5/58 (Item 36 from file: 2)
DIALOG(R)File 2:INSPEC

01592421 INSPEC Abstract Number: B80051679, C80033536
Title: A new algorithm for power system stability calculations
Author(s): Young-moon Park
Journal: Journal of the Korean Institute of Electrical Engineers vol.29, no.3 p.193-200
Publication Date: March 1980 Country of Publication: South Korea
CODEN: JKIEAJ ISSN: 0374-4876
Language: Korean Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: A new algorithm for power system transient stability calculations is developed which considers the nonlinear state equations of 8 state variables for each generator dynamics, exponential **load models** in respect to bus voltages for nonlinear loads, network equations expressed in terms of bus-injected **current sources** , various kinds of generator and transmission line outages, abrupt changes in loads, and operations of

various kinds of protective relaying systems. In the algorithm are included efficient and reliable schemes for solving network equations by means of the Newton-Raphson iterative method and the Optimally-Ordered Triangular Factorization Technique, and simple procedures for determining fault-point negative and zero sequence impedances for unbalanced line faults. The application of the Optimally-Ordered Triangular Factorization Techniques results in large savings of computing time and memory requirements. (3 Refs)
Subfile: B C
Descriptors: power system analysis computing; power system protection; stability; transients
Identifiers: power system stability calculations; algorithm; transient stability; nonlinear state equations; 8 state variables; nonlinear loads; line outages; protective relaying systems; zero sequence impedances; unbalanced line faults; computing time; memory requirements; bus injected **current sources** ; Newton Raphson iterative method; optimally ordered triangular factorisation method
Class Codes: B8110B (Power system management, operation and economics); B8110D (Power system planning and layout); C7410B (Power engineering)

36/5/59 (Item 37 from file: 2)
DIALOG(R)File 2:INSPEC

01560037 INSPEC Abstract Number: B80042048
Title: The European network
Author(s): Glavitsch, H.
Author Affiliation: ETH, Zurich, Switzerland
Journal: Elektrotechnik vol.31, no.4 p.77-80
Publication Date: May 1980 Country of Publication: Switzerland
CODEN: EKTKD6 ISSN: 0013-581X
Language: German Document Type: Journal Paper (JP)
Treatment: General, Review (G)
Abstract: Exchange of power between various countries of Europe through the **interconnecting grid** is considered by taking into consideration technical and economic aspects. The 420 kV and 245 kV transmission grids are described together with frequency control and failure occurrences. (0 Refs)
Subfile: B
Descriptors: frequency control; power system interconnection; transmission networks
Identifiers: Europe; **interconnecting grid** ; 245 kV transmission; frequency control; failure; 420 kV transmission power exchange
Class Codes: B8110B (Power system management, operation and economics); B8120E (a.c. transmission)

36/5/60 (Item 38 from file: 2)
DIALOG(R)File 2:INSPEC

00089171 INSPEC Abstract Number: B70005849
Title: Load flow fundamentals
Author(s): Green, R.K., Jr.; Bowen, J.L.; Mo-Shing Chen
Author Affiliation: Dallas Power & Light Co., Dallas, TX, USA
Conference Title: 21st annual Southwestern IEEE conference and exhibition p.8 pp.
Publisher: Institute of Electrical and Electronics Engineers, New York, NY, USA
Publication Date: 1969 Country of Publication: USA xiii+826 pp.
Conference Date: 23-25 April 1969 Conference Location: San Antonio, TX, USA
Language: English Document Type: Conference Paper (PA)
Abstract: Develops the basic physical and mathematical theories of node frame load flow. Special emphasis is placed on power system characteristics that have made the load flow problem and successive displacement iterative

solution techniques somewhat incompatible with one another. The node frame load flow is defined as a circuit analysis in which branch impedances and node power are known and node voltages and branch powers are calculated. The development of the load flow theory begins with generation and **load represented** as **current sources** .
Subfile: B
Descriptors: distribution networks; load (electric)
Class Codes: B8120 (Power transmission, distribution and supply)

36/5/61 (Item 1 from file: 95)

01339608 I99090122300
Whither LCOS? (liquid-crystal-on-silicon displays)
Mosley, A; Banks, L
CRL Hayes, UK
Information Display, v15, n4-5, pp14-17, 1999
Document type: journal article Language: English
Record type: Abstract
ISSN: 0362-0972

ABSTRACT:
Liquid-crystal-on-silicon displays have a very bright future-but there are several types, and each type is best suited to particular applications. At this time, the future of LCOS displays appears to be very promising. There are two potentially very large markets: rear-projection desktop monitors and viewers for mobile telephones, that can be addressed by LCOS technology. There are already some signs that manufacturers have realized that the transfer of very large amounts of data, particularly for the highly cost effective single- **channel display** systems, will be an issue. Consequently, SRAM silicon backplanes are being considered. While SRAM devices are ideally suited to driving fast-switching bistable FLC materials, they are not suited to the addressing of fast switching nematics. In order to drive the latter materials, circuitry is required that is able to store a frame of data at the pixel level and provide multiple voltage levels to obtain the required number of gray levels.

DESCRIPTORS: FERROELECTRIC LIQUID CRYSTALS; LCD--LIQUID CRYSTAL **DISPLAYS** ; **SRAM** CHIPS; MANUFACTURER; ELECTRONIC DEVICES; GRAY LEVEL
IDENTIFIERS: RECHNERBILDSCHIRM; SILICIUMFLUESSIGKRISTALL; GROSSMARKT; MOBILTELEFON; BETRACHTER; SILICIUMRUECKWANDPLATINE; Fluessigkristallanzeige ; Siliciumfluessigkristall

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Set     Items   Description
S1    7182620   MODEL? ? OR VISUAL? OR DIAGRAM? OR GRAPHIC? OR DISPLAY? OR
            CHART? OR REPRESENT? OR GRAPH? ?
S2          2   POWER()CONVERTER(N)S1
S3    8784741   PLURAL? OR VARIOUS OR SEVERAL OR MULTIPL? OR MANY OR NUMER-
            OUS OR UNLIMITED
S4      33791   (BOARD OR CONTROLLER)(N)S1
S5      16302   PACKAGE? (N)S1
S6      39125   (CHIP? ? OR MICROCHIP OR INTEGRATED()CIRCUIT? OR IC OR RAM
            OR RANDOM()ACCESS()MEMORY OR DRAM? OR SRAM? OR ROM? OR PROM? -
            OR EPROM? OR EEPROM? OR FLASH)(N)S1
S7    9910667   COMPRIS? OR INCLUDE? OR CONTAIN?
S8          0   (BUMP AND GRIND)(N)S1
S9       1216   LOAD(N)S1
S10      4727   CHANNEL(N)S1
S11    406788   (DC OR DIRECT()CURRENT) AND (DC OR DIRECT()CURRENT)
S12        23   VOLTAGE()CONTROL?()RESISTOR?
S13      3031   CURRENT()SOURCE?
S14        17   (INTERCONNECTING OR INTER()CONNECTING)()GRID?
S15         0   THREE()SECTION()GRID
S16        38   (BUMP OR GRIND)(N) S1
S17         0   S2 (S) S4 (S) S5
S18         0   S2 (S) S4
S19      3263   POWER()CONVERTER?
S20         0   S19 (S) S4 (S) S5
S21         1   S2 NOT PY>2001
File  15:ABI/Inform(R) 1971-2004/Jun 17
         (c) 2004 ProQuest Info&Learning
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 647:CMP  Computer Fulltext 1988-2004/Jun W1
         (c) 2004 CMP Media, LLC
File 275:Gale Group Computer DB(TM) 1983-2004/Jun 17
         (c) 2004 The Gale Group
File 674:Computer News Fulltext 1989-2004/Jun W2
         (c) 2004 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2004/Jun 16
         (c) 2004 The Dialog Corp.
File 624:McGraw-Hill Publications 1985-2004/Jun 16
         (c) 2004 McGraw-Hill Co. Inc
File 621:Gale Group New Prod.Annou.(R) 1985-2004/Jun 17
         (c) 2004 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2004/Jun 16
         (c) 2004 The Gale Group
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2004/Jun 17
         (c) 2004 PR Newswire Association Inc
File  16:Gale Group PROMT(R) 1990-2004/Jun 17
         (c) 2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 553:Wilson Bus. Abs. FullText 1982-2004/Jun
         (c) 2004 The HW Wilson Co
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